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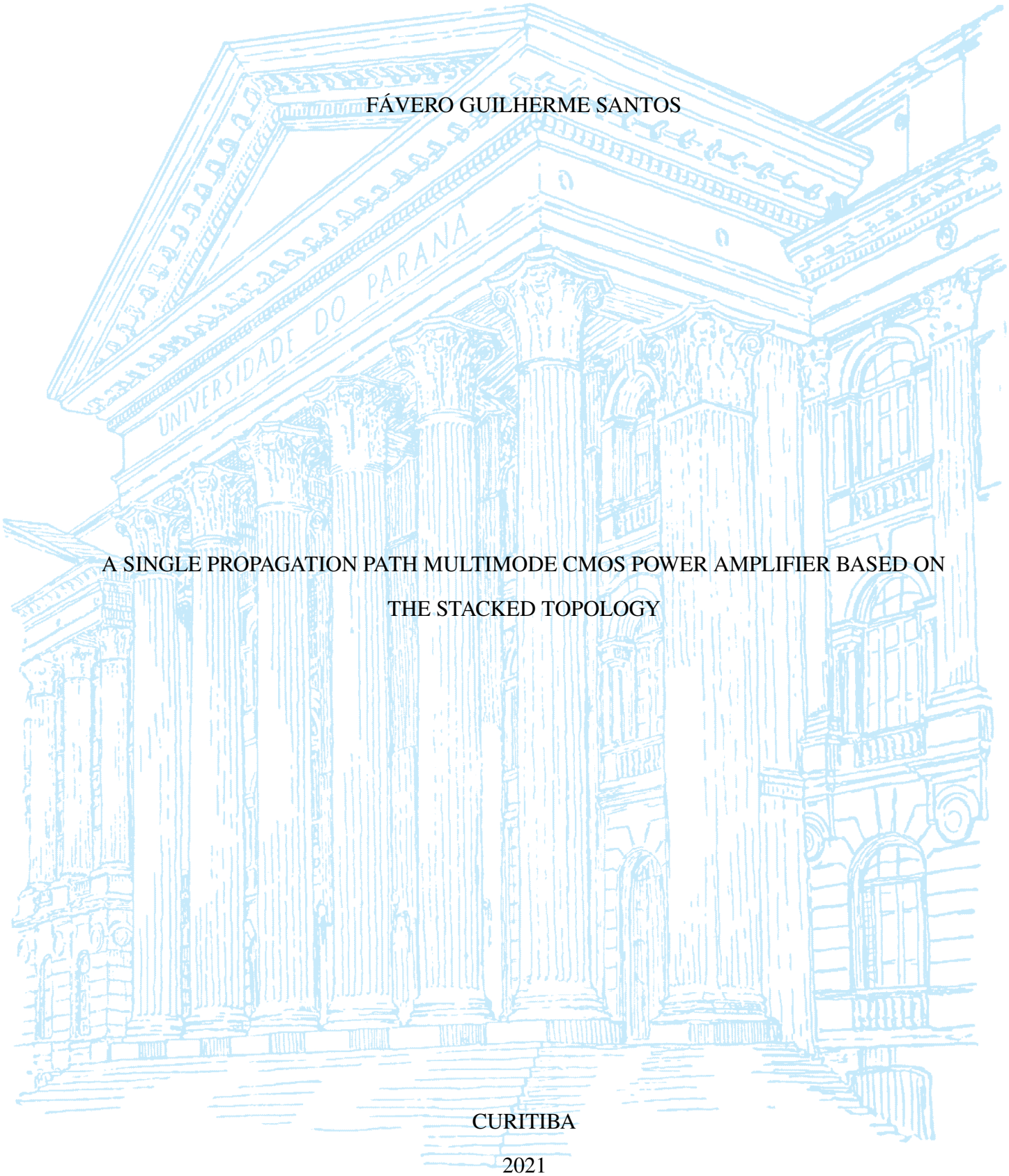


# A SINGLE PROPAGATION PATH MULTIMODE CMOS POWER AMPLIFIER BASED ON THE STACKED TOPOLOGY

CURITIBA

2021

FÁVERO GUILHERME SANTOS

# A SINGLE PROPAGATION PATH MULTIMODE CMOS POWER AMPLIFIER BASED ON THE STACKED TOPOLOGY

Tese apresentada ao Programa de Pós-Graduação em Engenharia Elétrica, setor de Tecnologia, Universidade Federal do Paraná, como requisito parcial à obtenção do título de Doutor em Engenharia Elétrica.

Orientador: Bernardo Rego Barros de Almeida Leite.

Coorientador: André Augusto Mariano.

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# APPROVAL MINUTE

The Examining Board is designated by the Faculty of the Graduate Program of the Federal University of Paraná in ENGENHARIA ELÉTRICA where invited to argue the DISSERTATION of PHILOSOPHY DOCTOR by **FÁVERO GUILHERME SANTOS** , entitled: **A single propagation path multimode CMOS PA based on the stacked topology**, under the supervision of Dr. BERNARDO REGO BARROS DE ALMEIDA LEITE, which and after assessment of the candidate and the work, the Examining Board decided for the APPROVAL in the present rite.

The granting of the title of philosophy doctor is contingent upon the fulfillment of all the requirements indicated by the Examining Board and terms determined in the regulation of the Graduate Program.

CURITIBA, June 28th, 2021.

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ERIC KERHERVÉ
External Member (BORDEAUX INP)

*To Talita, who is;*
*To Aurora, who was;*
*and to who will be -*
*personifications of love.*

*Present, past, and future.*

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to Talita Camargo, for her understanding and unconditional support,
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and finally, to my friends & family, who never stopped believing in me.

## RESUMO

Esta tese apresenta o projeto de um amplificador de potências (PA) prova-de-conceito com quatro perfis de eficiência de um caminho único de propagação, realizado com tecnologia CMOS 130 nm e operando em 2,4 GHz. Esse circuito se baseia em dois conceitos: na seleção da região de operação de transistores (triodo ou saturação) e na alteração da tensão de alimentação de uma arquitetura empilhada modificada. Nos modos de alta e baixa potência (todos transistores em saturação e um transistor em saturação e três em triodo, respectivamente), o ponto de compressão de 1 dB referenciado à saída ($OCP_{1dB}$) e a eficiência adicionada à potência (PAE) no $OCP_{1dB}$ resultantes de simulação pós-layout são de 19,9 dBm e 25,7%; de 15,1 dBm e 20,5%, respectivamente. Para validar a operação desse PA, quatro tipos de sinais do padrão IEEE 802.11ax foram testados. Para sinais menos complexos (16 QAM) o PA pode operar sem que a ultrapasse os limites impostos pela máscara do padrão até uma potencia de saída ($p_{out}$) de 17,8 dBm; para sinais mais complexos (1024 QAM) o PA pode operar até uma $p_{out}$ de 8,5 dBm. Por um lado, o circuito apresentado é capaz de ocupar uma pequena área, o que é uma vantagem em processos escaláveis, tais como o CMOS. Por outro lado, a complexidade de design é elevada, tendo em vista que a otimização de eficiência e potência é também função da interação entre os modos de operação.



Palavras-chave: Amplificador de potências CMOS em 2,4 GHz. Amplificador de potências RF CMOS. Amplificador de potências multimodo. Amplificador de potências reconfigurável. Amplificador de potências empilhado.

## ABSTRACT

This thesis presents the design of a proof-of-concept single propagation path four-mode power amplifier (PA) in 130 nm CMOS operating at 2.4 GHz. It is based on two concepts: the selection of the transistor's operation region (triode or saturation) and on the scaling of supply voltage of a modified stacked architecture. In high and low power modes (all transistors in saturation and one transistor in saturation and three in triode, respectively), the output-referred 1 dB compression point ($OCP_{1dB}$) and the power added efficiency (PAE) in $OCP_{1dB}$ post-layout simulation results are 19.9 dBm and 25.7%; 15.1 dBm and 20.5%, respectively. To validate this PA's operation capability, four types of IEEE 802.11ax signals were tested. For less complex signals (16 QAM) the PA can operate without exceeding the limits imposed by the standard's mask up to an output power ($p_{out}$) of 17.8 dBm; for more complex signals (1024 QAM) the PA can operate up to a $p_{out}$ of 8.5 dBm. On the one hand, the proposed circuit is capable of occupying a small area, which is an advantage in scalable processes, such as CMOS is. On the other hand, its design is complex, as optimization of efficiency and power is also a function of the interaction among operation modes.



Keywords: 2.4 GHz CMOS power amplifier. RF CMOS multimode power amplifier. Multimode power amplifier. Reconfigurable power amplifier. Stacked power amplifier.

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## LIST OF ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| ac | Alternating current |
| ACPR | Adjacent Channel Power Ratio |
| AMCP | Average Main Channel Power |
| CG | Common Gate |
| CMOS | Complementary Metal Oxide Semiconductor |
| CS | Common Source |
| dc | Direct current |
| DRC | Design Rule Check |
| EVM | Error Vector Magnitude |
| FET | Field Effect Transistor |
| GDS | Graphic Design System |
| IEEE | Institute of Electrical and Electronics Engineers |
| LVS | Layout Versus Schematic |
| MCS | Modulation Coding Scheme |
| MIM | Metal-Insulator-Metal |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| $OCP_{1dB}$ | Output Referred 1 dB Compression Point |
| OSI | Open Systems Interconnection |
| PA | Power Amplifier |
| PAE | Power Added Efficiency |
| PEx | Parasitic Extraction |
| PHY | Physical |
| PSD | Power Spectrum Density |
| PVT | Process Voltage Temperature |
| pp | Percentage point |
| QAM | Quadrature Amplitude Modulation |
| RF | Radio Frequency |
| RMS | Root Mean Square |

## LIST OF SYMBOLS

| | |
|---|---|
| A | Ampères |
| $A_{vo}$ | Open loop voltage gain |
| $C_{gs}$ | Gate-source intrinsic capacitance |
| $C_i$ | Gate capacitance at the $i^{th}$ position |
| $g_m$ | Small-signal gate transconductance |
| $g_{sd}$ | Small-signal source-drain transconductance |
| $R_{DS}$ | Triode operation drain-to-source resistance |
| $R_o$ | Open loop output resistance |
| $R_{opt}$ | Optimum load line resistance |
| S | Siemens |
| V | Volts |
| $V_{DC}$ | Supply voltage |
| $V_{MAX}$ | Maximum allowed voltage |
| $Z_{loadpull}$ | Load-pull impedance |
| W | Watts |
| Ω | Ohms |

## DEFINITIONS AND NOTATIONS

### Definitions

| | |
|---|---|
| $p_{in}$ | RMS value of the power inputted to the amplifier |
| $p_{out}$ | RMS value of the power outputted by the amplifier |
| $p_{sat}$ | RMS value of the saturated output power |
| $p_{max}$ | RMS value of the maximum power outputted by the amplifier when efficiency reaches its maximum |
| $P_{DC}$ | is equal to $V_{DC}$ times $I_{DC}$ |
| PAE | is equal to $(p_{out} - p_{in}) / P_{DC}$ |

### Notations

| | |
|---|---|
| i | A dc only voltage/current is represented by uppercase letter(s) followed by uppercase subscript letter(s). Example: a dc voltage drop across the gate and source of a transistor is represented by $V_{GS}$. |
| ii | An ac only voltage/current is represented by lowercase letter(s) followed by lowercase subscript letter(s). Example: an ac voltage drop across the gate and source of a transistor is represented by $v_{gs}$. |
| iii | A combined dc and ac voltage/current is represented by uppercase letter(s) followed by lowercase subscript letter(s). Example: a combined dc and ac voltage drop across the gate and source of a transistor is represented by $V_{gs}$. |

Examples of such notations are presented in Figure 1.

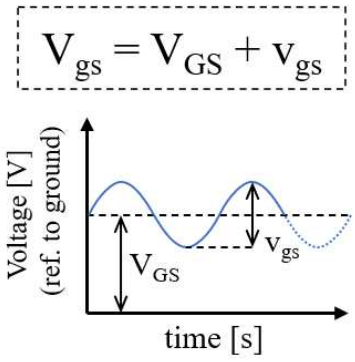


Figure 1: Examples of notations employed in this work.

**CONTENTS**

# 1 INTRODUCTION

## 1.1 OPPORTUNITIES AND CHALLENGES

THE transmit power control is a feature of the high-efficiency standard IEEE 802.11ax which allows the dynamic decrease of output power ($p_{out}$) levels. Although this mechanism is primarily intended to reduce interference (Bellalta, 2016) among devices by increasing spatial reuse, at the PHY level it can be employed to optimize overall efficiency of the transmission system if the reduction of $p_{out}$ results in the increase of efficiency. There is, however, a problem with this assertion: there is a well-known trade-off between linearity and efficiency in power amplifier (PA) design (Ruiz and Pérez, 2014; McCune, 2015a). How to overcome this nonintuitive scenario? One possible way is to employ the multimode PA architecture.

Multimode PAs are circuits capable of operating in different efficiency profiles (or modes). When compared among themselves, these patterns emphasize the PA's capacity of achieving distinct efficiencies for a fixed $p_{out}$. Differently from single mode PAs, which have only one efficiency profile (Figure 1.1-A), multimode PAs have at least two efficiency profiles (Figure 1.1-B). Consider, for example, the output power of a single mode PA to be equal to the $p_{out1}$ of a multimode PA. In the former case, as there is only one efficiency profile, $PAE_{EP1}(p_{out1}) = PAE_1$ (PAE stands for Power Added Efficiency, a metric for measuring efficiency in PAs). In the later case, the architecture allows the selection of the highest efficiency curve, and, thus, $PAE_{EP2}(p_{out1}) = PAE_2 > PAE_1$. It is important to observe that such curves should be horizontally spaced between themselves as it translates an efficient usage of the PA's $p_{out}$ dynamic control range. Inversely, it is not desired these curves to be horizontally around the same center as this scenario would translate into unusable efficiency curves, although multimode operation occurs.

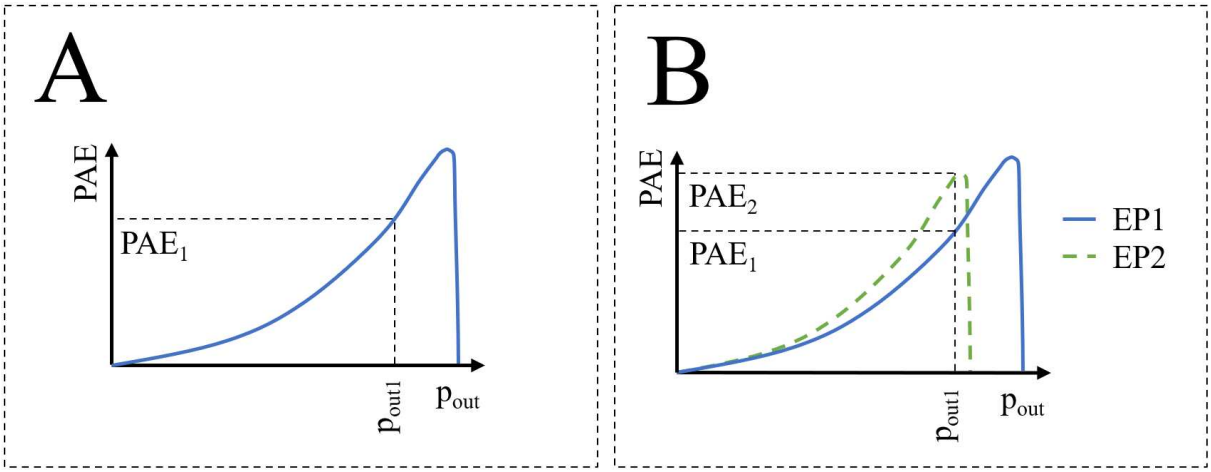


Figure 1.1: Single mode (A) and multimode (B) PA efficiency profiles. If $p_{out1}$ is fixed for both scenarios, $PAE_2$ is greater than $PAE_1$ because a more efficient profile can be selected for the intended output power.

Multimode operation can either be obtained when the RF signal flows through one (single propagation) or multiple signal (multi-propagation) paths.

Multi-propagation multimode PAs are systems in which the RF signal is relayed or divided to parallel amplification cores, as depicted in Figure 1.2-B (McCune, 2015b). Non exhaustive examples of such architectures are presented in Modesto et al. (2019), Tarui et al. (2018), Luong et al. (2018), Ou et al. (2017), Santos et al. (2016), and An et al. (2009). Single

propagation multimode PAs, in their turn, are systems capable of achieving multimode operation without relaying or dividing the RF signal to other parallel amplification cores (Figure 1.2-A), as presented in Santos et al. (2020), Huang et al. (2017), and Hsieh and Tsai (2017).

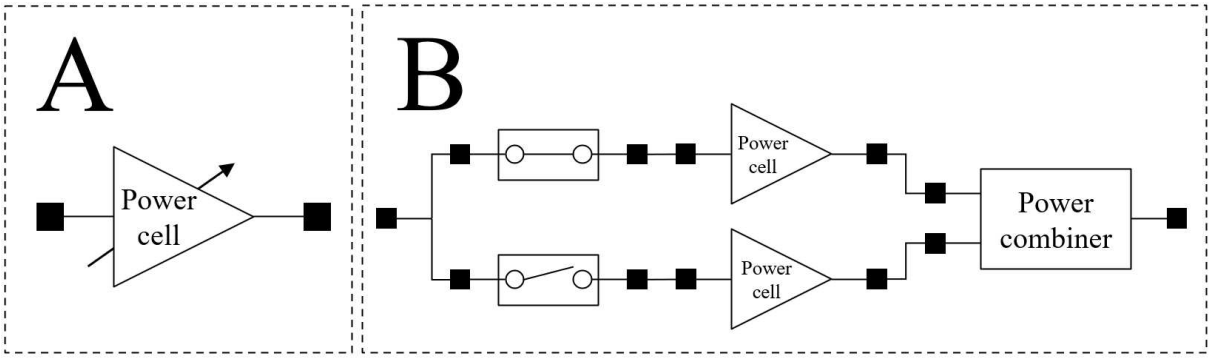


Figure 1.2: Examples of a single propagation path multimode PA (A) and of a multi-propagation path multimode PA (B). In A, multiple efficiency profiles are obtained via a variable power cell and in B, multimode operation is obtained by combining individually the $p_{out}$ of each fixed cell.

The multi-propagation path is a configuration more frequent in the literature partly because achieving multiple efficiency profiles via parallel power structures is a natural idea. For example, a multitude of modes can be easily obtained if a power structure is designed, replicated, and made somehow capable to be turned on and off when more or less power is needed (e.g., the sixty four mode PA presented in Tarui et al. (2018)). The main issue, however, is how to combine the outputs of each power cell is such a manner that efficiency is minimally degraded by the presence of a power combiner's parasitics (such as those present in transformers, baluns, switches or passive networks) (inset B of Figure 1.2).

In this context, there is interest in developing single propagation multimode PAs because this architecture avails from not employing power combiners at the output nor using switches at the input (or output) of the power structures (inset A of Figure 1.2), and it allows a more compact layout as a reduced amount of elements is needed. However, all these advantages come at a cost of a complex optimization of the design, as the amplification of the signal depends on how well the path's elements interact with each other.

Apart from the discussion of pros and cons of such architectures, another aspect of interest for CMOS PAs design is the intrinsic low breakdown voltage (Ruiz and Pérez, 2014; Tsividis, 2013) that limits the $p_{out}$ of an amplifier. This situation is of special care for traditional architectures (such as the common-source (CS)) because the supply and ground rails are connected directly to the amplification core - meaning that the selection of supply voltage ($V_{DD}$) is significantly restricted by the employed technology. In this thesis the breakdown voltage limit was translated to a parameter of the employed device: the maximum allowed voltage ($V_{MAX}$).

It may seem that CMOS PAs are fated to an ever reducing power performance as processes scale down but this vision does not consider the ingenuity of composite architectures, such as those which result from the process of vertically series-connecting devices. By stacking devices, each transistor of the stack divides the strain of a high $V_{DD}$ (Tarar et al., 2016; Dabag et al., 2013; Pornpromlikit et al., 2010). For example, a stack of two transistors can withstand a $V_{DD}$ of 3 V even if $V_{MAX}$ equals to 1.6 V (in this situation, each transistor will have to deal with a voltage drop of 1.5 V, for example).

Although the stacked architecture solves the issue of power performance, the reader may have noticed that this type of series connection is intrinsically a single propagation path single mode PA architecture. But what if it could be transformed into a multimode one?

## 1.2 HYPOTHESIS AND OBJECTIVES

Considering the potential of multimode PAs and the advantages of single propagation architectures, the following hypothesis is conjectured:

> It is possible to achieve multimode operation in a stacked architecture if the transistors in the stack may be operated either as closed switches or amplifiers depending on the aimed $p_{out}$. In this sense, if the number of amplifiers in the stack increases, the available $p_{out}$ increases; inversely, if the number of closed switches in the stack increases, the available $p_{out}$ decreases. The efficiency of this architecture is function of the behavior of the transistors and the supply voltage applied to it.

To verify this conjecture, this work's general objective is to present and to discuss the obtained post-layout simulation performance of a proof-of-concept single propagation path multimode PA. In terms of specific objectives, this thesis will focus on the discussions of the supporting concepts of the application of such circuit, the review of literature concerning multimode CMOS PAs, the discussion of the theory that supports the stacked configuration, and the expansion on it to explain the details of the proposed circuit configuration. Additionally, other specific objectives of this work are: to address circuit design and layout constraints, to present the performance of such circuit under process, voltage and temperature variations, and, lastly, to present simulations regarding continuous-wave and modulated sources.

## 1.3 CONTRIBUTIONS

The contributions of this work regard to the theoretical review of the common-source, cascode, and stacked architectures considering a crucial design aspect, reliability. It also contributes by proposing a comparison of recent works found in the literature by summarizing which architectures and techniques are employed to obtain multimode operation for PAs. Additionally, it expands the knowledge in the field of application of PA design by proposing an architecture named in this work as hybrid. Besides discussing essential matters of electronic circuits for this circuit's characterization, this work also expands the knowledge basis by proposing a taxonomy in the field of multimode PAs.

In terms of scientific contributions, the following works were developed during this doctorate studies:

- Santos, F. G., Leite, B. R. B. de A., and Mariano, A. A. (2021). A Multimode CMOS PA with a Single Propagation Path. ALOG - Analog Integrated Circuits and Signal Processing, Springer, v. 108, pp. 421-435.

- Rocha, P., Santos, F. G., B. R. B. de A., and Mariano, A. A. (2021). An 130 nm CMOS Cascode PA with Linearity and Efficiency Enhancement based on Body Effect. In 2021 $27^{th}$ Iberchip Workshop.

- Santos, F. G., Leite, B. R. B. de A., and Mariano, A. A. (2020). A novel single propagation path multimode PA. In 2020 33rd Symposium on Integrated Circuits and Systems Design (SBCCI). Institute of Electrical & Electronics Engineers (IEEE).
- Modesto, A., Santos, F., Pereira, J., Leite, B. and Mariano, A. (2019). A CMOS power amplifier with reconfigurable power cells and matching network for 2.4 GHz wireless communications. AEU - International Journal of Electronics and Communications, Elsevier BV, v. 111, n. 152919.

## 1.4 THESIS ORGANIZATION

The reader is invited to follow this thesis through the theoretical foundation (Chapter 2) where common PA architectures such as the common-source, cascode, stacked, and a multimode version of the last one, the hybrid, are discussed. Not only limited to the hybrid, these architectures are employed with other techniques (such as supply voltage scaling or power cell selection) to provide PAs with multimode capability. Later on, based on the principles laid out in the Section 2.3 and expanding on the state-of-the-art, this work presents the design of a proof-of-concept CMOS PA (Chapter 3), its post-layout simulation results, and the comparison to selected works (Chapter 4). Finally, all concepts and results of this work are wrapped up in the Conclusion.

# 2 THEORETICAL FOUNDATION

In this chapter, selected PA design topics such as architectures, operation, constraints, and a review of the state-of-the-art of multimode CMOS PAs will be presented. Specifically, it will focus on discussing the outcomes of vertically series connecting transistors, a technique know as stacking. Examples of such topologies are the cascode, the stacked, and that presented in this thesis, the hybrid. A characteristic that they all share in common is their common-source (CS) input stage. Apart from that, the subsequent amplifiers of the cascode are in common-gate (CG) configuration (so no signal swings are present at the gates) while in the stacked they are not (so signals swings are present at each gate). Finally, the hybrid is the stacked architecture that relaxes the amplifier operation constraint, allowing transistors to also behave as closed switches, and thus, allowing multimode operation.

The equations presented in this chapter are based on the low frequency, four terminal, simplified small-signal model for MOSFET available in (Tsividis, 2013). In general, all parasitics capacitances will be zeroed; in such situations, it is considered that the frequency of operation of the circuit is well bellow the maximum transition frequency. In order to explain some ac effects, the intrinsic gate-to-source capacitance ($C_{gs}$) will be considered, but when this happens, it will be clearly stated. Finally, drain-to-source and body-to-source currents will all be equal to zero and source and body terminals are shorted.

## 2.1 THE CASCODE CONFIGURATION

As stated before, the typical cascode arrangement is a topology in which lower amplifier is in CS configuration while the upper in CG so the stack height *n* is equal to two. The CS is responsible for amplifying the input and the CG to buffer and isolate the current to/from the output. To achieve CG in the upper transistor, a large gate capacitance ($C_1$) is placed in such a manner that ac voltages are filtered to ground. Usually, the gate of the CG is biased with a voltage equal to the supply voltage (Ruiz and Pérez, 2014).

Stacking devices in the cascode amplifier is an interesting technique to deal with some limitations of CS amplifiers (Figure 2.1-A) in CMOS technology: output resistance ($R_o$), open-loop voltage gain ($A_{vo}$), and $p_{out}$.

Firstly, low output resistance is an issue because it leads to a low transformation ratio between load and the $R_o$ of amplifier; the lower the transformation ratio, the more inefficient the amplified signal is transmitted to the load, and, in overall, the more inefficient the PA is (Ruiz and Pérez, 2014). Differently from the CS where the $R_o$ equals $1/g_{sd0}$, the $R_o$ of the cascode is $((g_{sd0} + g_{m1})/g_{sd0} \cdot g_{sd1})$ higher (Razavi, 2013), as presented in Equation 2.1.

$$R_o\big|_{cascode} = \frac{1}{g_{sd0}} + \frac{g_{sd0}+g_{m1}}{g_{sd0} \cdot g_{sd1}} \tag{2.1}$$

Secondly, the $A_{vo}$ of the cascode is $(1 + g_{m1}/g_{sd1})$ times greater than the gain of a CS amplifier ($-g_{m0}/g_{sd0}$, (Razavi, 2013), presented in Equation 2.2): the higher the $A_{vo}$ is, the higher it is the peak $v_{out}$. Finally, with a higher peak $v_{out}$, a higher $p_{out}$ is achievable. This increased $p_{out}$, however, can be only supported by the more complex voltage distribution in the structure, as the comparison of the Figures 2.2-B and 2.1-B shows. Additionally, as the cascode has a

high reverse isolation ($|S_{12}|$), this circuit has less feedback and, thus, is more stable than the CS amplifier (Razavi, 2011).

$$A_{vo}\Big|_{cascode} = -\frac{g_{m0}}{g_{sd0}} \cdot \left(1 + \frac{g_{m1}}{g_{sd1}}\right) \tag{2.2}$$

In terms of oxide breakdown reliability, the voltages that should be considered cautiously for the CS are the instantaneous drain-to-gate ($\hat{V}_{dg}$) and drain-to-source ($\hat{V}_{ds}$) voltages, which both must be lower than $V_{MAX}$. These voltages limit the peak drain voltage, and consequently, limit output power capability. In the cascode, however, a higher peak drain voltage is achievable because the voltage at node VD1 follows the voltage at node VD0; in so happening, the designer should maintain the instantaneous drain-to-drain between M1 and M0 ($\hat{V}_{d1d0}$) and drain-to-gate ($\hat{V}_{d1g1}$) voltages lower than $V_{MAX}$. Observe that the requirements of oxide breakdown in the cascode are accumulative in regards to the CS, so the reliability should be met at both CS and CG levels.

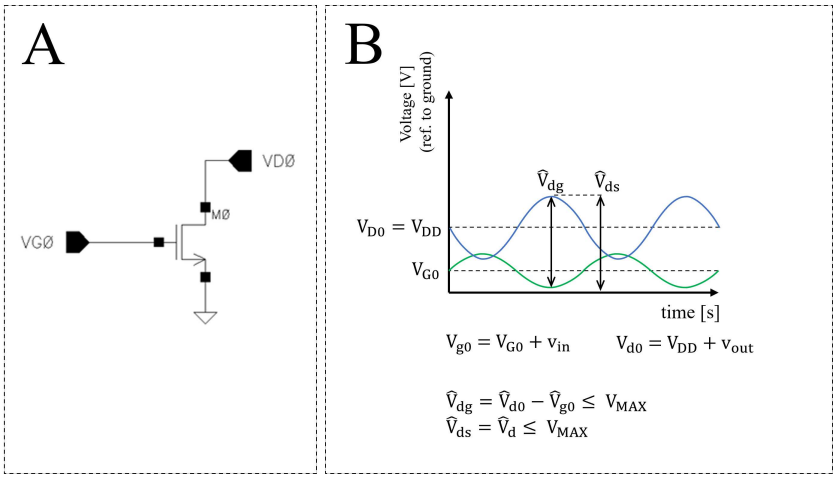


Figure 2.1: (A) The CS amplifier topology. (B) Voltage distribution in a class A CS amplifier.

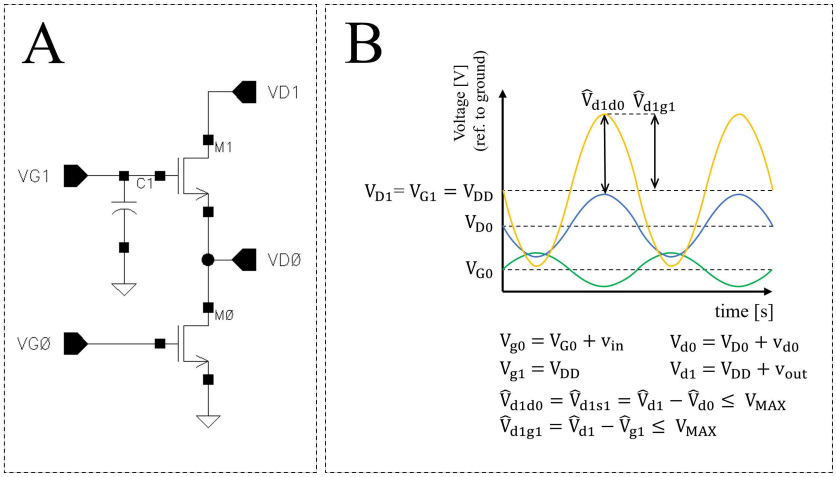


Figure 2.2: (A) The cascode amplifier topology. (B) Voltage distribution in a class A cascode amplifier.

Although the previous discussion considers a cascode of $n$ equals two, one may understand the "cascoding" process as the building up of CG amplifiers atop of the CS amplifier,

or, in other words, not limiting the cascode to *n* equals two. An example of such idea is presented in Luong et al. (2018) where a tripple-cascode CMOS PA is discussed. This configuration allows, in the same sense as even higher stack height allows, the usage of a high supply voltage while keeping transistors low breakdown voltage checked, and thus, achieving high $p_{out}$ even in scalable CMOS processes.

Lastly, the cascode amplifier is one of the sustaining pillars of the multi-propagation path multimode PA domain. This so happens because the CG cell can be easily turned off (cut-off operation) and on by applying or not biasing voltage at the CG. Adequately, when in off state, the output resistance increases drastically (it becomes as high as a CMOS off-switch) and, ideally, no signal is fed back into the structure. This characteristic is of special interest when multiple cascode amplifiers are employed in parallel and tied to a common load: when selecting which of those cells are enabled or disabled, multimode operation is achieved. Examples of such usability will be presented in Section 2.4.

## 2.2 THE STACKED CONFIGURATION

Much like the cascode, the stacked is also an arrangement of vertically series-connected transistors with height *n* differing from the former by not having ac voltages at the gates of each stacked transistor. This association is made when the drain of a lower position transistor is shorted to the source of a higher position transistor. If the transistor's index (*i*) in the stack is zero, the transistor's source is grounded. If *i* is equal to (*n* - 1), the transistor's drain is connected to the supply voltage ($V_{DD}$) usually through a choke inductor. An example of such configuration with *n* equals three (M0, M1, and M2) is presented in Figure 2.3-A.

Other essential components in this circuit are the gate capacitors ($C_i$ - *e.g.*, C1 and C2 of Figure 2.3-A) which are connected between the gate and the ground rail in every *i* greater than zero up until (*n* - 1). Together with the $C_{gs}$, they act as ac voltage dividers and are employed to control the magnitude of the voltage swing between gate and source terminals (Pornpromlikit et al., 2010; Dabag et al., 2013). Additionally, they are also important to adjust the impedance at each drain of the stack and to keep the voltage swings bellow the $V_{MAX}$ (Tarar et al., 2016).

There can be found at least two analytical methods in the literature to determine the gate capacitance values for the stack. They are both based on the analysis of a low-frequency small-signal simplified model for MOSFET and differ on the amount and type of considered passives. The premise for such evaluations is the resistance matching between the $i^{th}$ transistor drain (which has the load line resistance $R_{OPT}$ equals to $V_{DS}$ by $I_{DS}$) to the source drain of the ($i^{th}$-1) transistor. By doing so, voltages are effectively added in phase at each level of the stack, providing a higher voltage swing at the top of the stack, and thus, a higher $p_{out}$ and gain, if compared to unmatched condition.

The first analytical method is presented in Equation 2.3 from Dabag et al. (2013) while the second one, a simplified version of such equation where only $C_{gs}$ is considered, is presented in Kim and Kwon (2015). As stated before, these methods are based on simplified, low-frequency, small-signal models and thus, their validity may be questioned at high-frequencies and large-signal operation (Kim et al., 2011).

$$C_i = \frac{C_{gs}+C_{gd}\cdot(1+R_{OPT}\cdot g_m)}{(i-1)\cdot g_m\cdot R_{OPT}-1} \tag{2.3}$$

With $i \in 2 < \mathbb{N} < n$.

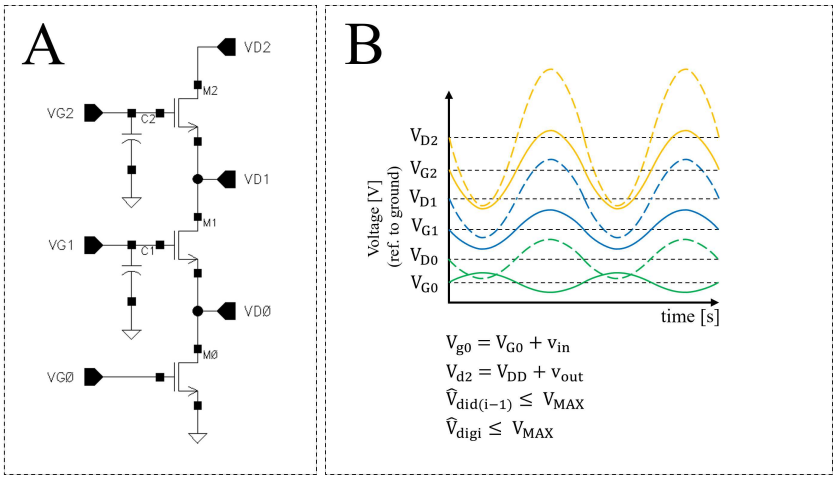


Figure 2.3: (A) The stacked amplifier topology. (B) Voltage distribution in a class A stacked amplifier.

A third method is based on recursive (supervised or not) optimization of C1 and C2 based on the analysis of an established set of metrics (such as efficiency, linearity, or gain, for example) to select the proper capacitance values. To do so, several simulations are ran, each one of them with different values of capacitances, and the effects of such variations are registered. Based on the obtained results, the designer must ponder and decide which values are the best suited for the intended application. Differently from the previous simplified methods, this approach considers the full model of the transistor and non-linear effects, and, thus, provides the most accurate results.

Even tough not shown in Figure 2.3-A, the biasing sources must have an impedance high enough in such way that no signal flows from the gate to such voltage sources. A way to do so is to place inductors (which may or may not be external components) between bias sources and the gate capacitors. Another way is to use a self-biased architecture such as that described in Ezzeddine and Huang (2003); Ezzedline and Huang (2000).

With regard to operation, all transistors in the stack operate exclusively as amplifiers. Its operation principle is to avail the consecutive in-phase amplifications produced by transistors in the stack, allowing the signal to be gradually amplified until it reaches the final drain terminal, where the power is delivered to the load (Tarar et al., 2016). This situation is depicted in the inset B of Figure 2.3.

As for reliability, any instantaneous voltage drop between device's terminals ($\hat{V}_{ds}$ or $\hat{V}_{gs}$, for example) must be lower than the $V_{MAX}$ in every transistor in the stack. Observe, however, that $\hat{V}_{ds} = V_{DS} + \hat{v}_{ds}$ which means that $V_{MAX}$ must accommodate not only the time varying signal, but also the dc portion.

In the same sense of the cascode, stacking is an useful technique as it presents an increasing $R_o$ (Equations 2.4, 2.5, and 2.6) and $A_{vo}$ (Equation 2.7) as the stack height increases.

$$R_o\big|_{n=1} = R_o\big|_{CS} = \frac{1}{g_{sd0}} \tag{2.4}$$

$$R_o\big|_{n=2} = R_o\big|_{cascode} = \frac{g_{sd0}+g_{sd1}+g_{m1}}{g_{sd0}\cdot g_{sd1}} \tag{2.5}$$

$$R_{o_n} = \frac{1}{g_{sd0}} + \left(\frac{g_{sd0}+g_{sd1}+g_{m1}}{g_{sd0}\cdot g_{sd1}}\right) \cdot \prod_{i=2}^{n-1}\left(1 + \frac{g_{mi}}{g_{sdi}}\right) \tag{2.6}$$

For $n \geq \mathbb{N} > 3$.

$$A_{vo_n} = \frac{-g_{m0}}{g_{sd0}} \cdot \prod_{i=1}^{n-1}\left(1 + \frac{g_{mi}}{g_{sdi}}\right) \tag{2.7}$$

For $n \geq \mathbb{N} > 2$.

Additionally to the presented design guidelines, careful thought should be considered when employing large values of $n$ as transistor parasitics causes phase variations at each drain of the stack (Montaseri et al., 2018), (Kim and Kwon, 2015) and the last transistor's drain to bulk voltage may be higher than the value rated by the employed process (Ruiz and Pérez, 2014). Optimal stack height resides between three and five (Montaseri et al., 2018).

In order to design such architecture reliably, some guidelines are available in Pornpromlikit et al. (2010), Dabag et al. (2013), and Tarar et al. (2016) discussing on how to select the voltage across every transistor in the stack. Expanding on previous works, this thesis proposes a variant method which will be explained on the following paragraphs and employs the value of $V_{MAX}$ as the principal design parameter. Furthermore, it is also important to note that it is possible to optimize such voltages to enhance either efficiency or linearity.

The first parameter is to select the dc drain to source voltage drop across every transistor ($V_{DS}$). An approach is to select this value by employing $V_{DS} = V_{MAX}/2$. This idea considers that the peak-to-peak value of $v_{ds}$ may be equal to $V_{DS}$ but their sum still lower than $V_{MAX}$. The voltage at every drain ($V_{Di}$) should follow the relation presented in Equation 2.8.

$$V_{Di} = (i + 1) \cdot V_{DS} \tag{2.8}$$

With $i \in 0 < \mathbb{N} < n - 1$.

In regards to the dc gate to source voltage drop across every transistor $V_{GS}$, this value should be selected based on the desired operation class of the amplifier. Then, to bias the transistors in the stack, Equation 2.9 should be used.

$$V_{Gi} = i \cdot V_{DS} + V_{GS} \tag{2.9}$$

With $i \in 0 < \mathbb{N} < n - 1$.

$V_{DD}$ is obtained when $i$ reaches position ($n$ - 1) (Equation 2.10).

$$V_{D(n-1)} = n \cdot V_{DS} = V_{DD} \tag{2.10}$$

## 2.3 THE HYBRID CONFIGURATION

In this section, the single propagation path multimode topology based of the stack arrangement (named in this thesis as hybrid) will be discussed. The main novelty that the hybrid establishes is that transistors in the array may operate as amplifiers (saturation) or as closed switches (triode),

depending on the selected biasing voltage. This selection allows the structure to operate rather as a single path multimode amplifier instead of a single path single mode architecture.

From the architectural perspective, the hybrid is very similar to the stacked: it is composed of vertically series-connected transistors with height $n$. Of these devices, $a$ of them behave as amplifiers while $s$ of them operating as closed switches, in such a manner that $n$ equals $a$ plus $s$. Considering the indexers $a$ and $s$, the configuration and efficiency profile of the hybrid may be designated by an univocal triplet in the format NnSsAa. For example, a hybrid described by N3S1A2 is composed of three stacked transistors, where one of them operate as a closed switch and two of them as amplifiers.

However, differently from the stacked, there are switches (S1 and S2 in Figure 2.4-A) in series with the gate capacitances (C1 and C2) which may be opened or closed, depending on the selected efficiency profile. This situation is depicted in Figure 2.4-B which presents the ac voltage distribution of the N3S1A2 configuration. Observe that $V_{d1}$ and $V_{d2}$ are equal, showing the closed switch behavior of M2 while other transistors behave as amplifiers. When selecting the capacitance values C1 and C2, one should have in mind that the total capacitance at the gate is the sum of the switch's capacitance in series with the gate capacitance.

The multimode operation of the hybrid is based on two main ideas: on the scaling of the supply voltage as modes are selected and on the change of region of operation from saturation to triode of a transistor by changing their biasing voltages. For example, if the last transistor of a stacked PA operates as a closed switch instead of an amplifier (inset B of Figure 2.4), lower output power will be achieved if compared to a stack where all transistors operate as amplifiers and $V_{DD}$ is at its maximum (inset A of Figure 2.4). Consecutively, if the last and penultimate transistors operate as closed switches instead of amplifiers and supply voltage is scaled down, even lower output powers are achievable (Figure 2.4-C). In conclusion, if the number of transistors operating as amplifiers increase, so should the supply voltage. Inversely, if the number of transistors operating as amplifiers decreases, so should the supply voltage. This notion is core to distinct this structure from the stacked arrangement and from other single propagation path configurations.

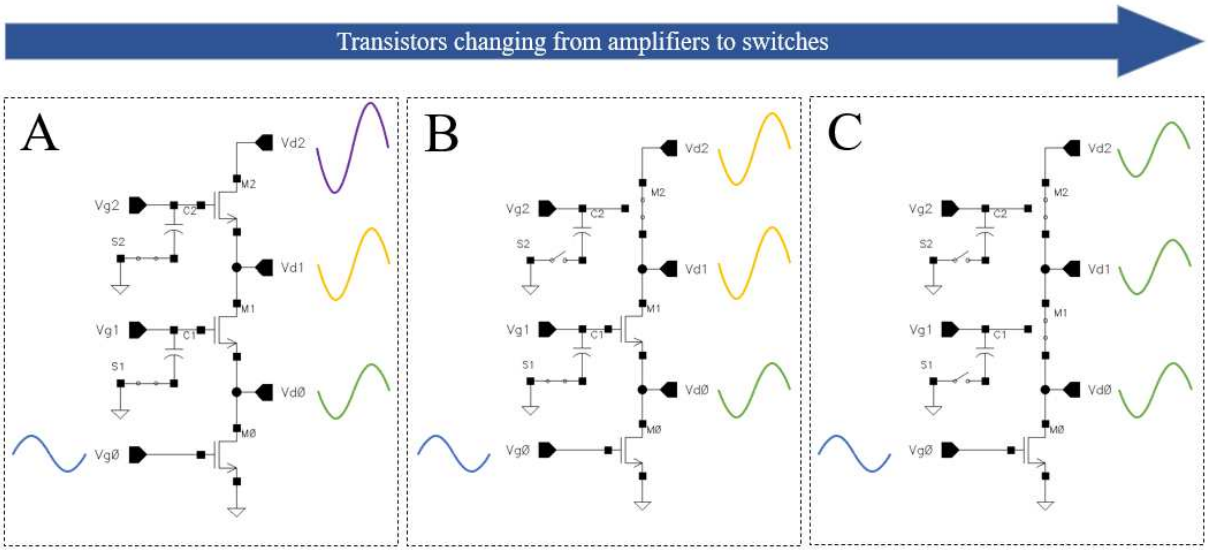


Figure 2.4: Example of how the hybrid multimode PA works. In (A) all transistors operate as amplifiers. In (B) M2 operates as a closed switch and M1 and M0 as amplifiers. Finally, in (C) M2 and M1 both operate as closed switches and M0 as an amplifier. $p_{out}$ reduces as transistors change from amplifiers to closed switches and as supply voltage is scaled down.

A detailed example of how voltage swings behave in a N3S2A1 configuration is presented in Figure 2.5-B. At $V_{g0}$, input voltage is applied to the gate of M0. As M0 is in CS configuration, $V_{dT0}$ is inverted. $V_{d0}$, then, is amplified via M1 and M2. As the last transistor operates as a closed switch, $V_{d3}$ is a copy of $V_{d2}$. $V_{g3}$ is set in such a manner that $V_{G3}$ voltage is enough to make the last transistor operate as closed switch and $v_{g3}$ is equal to $v_{d2}$.

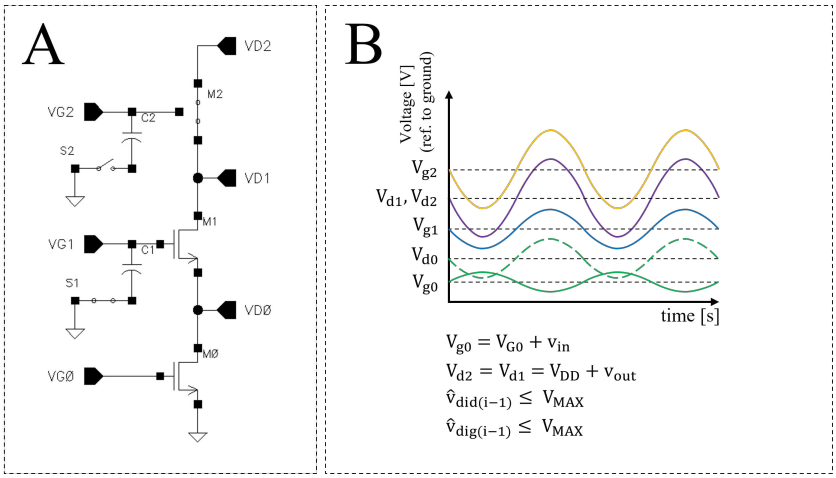


Figure 2.5: (A) The hybrid amplifier topology. (B) Voltage distribution in a class A hybrid amplifier.

In respect of the output resistance, the hybrid achieves its highest when NnS0An, which corresponds to the stacked configuration. For example, when N3S0A3, $R_o$ of the hybrid becomes equal to the output resistance of the stacked with *n* equals three (Equation 2.11). As efficiency modes change, the output resistance changes, as Equations 2.12 and 2.13 respectively show for N3S1A2 and for N3S2A1. This reduction of impedance happens firstly because there is no interaction between $g_{mi}$ and $g_{sdi}$ (as show in Equation 2.6) and due to the source-to-drain resistances when in triode (being $R_{DS_{Ti}}$ lower than $1/g_{sdi}$). Furthermore, observe that this dynamic increase or decrease of the output resistance directly affects on the selection of the optimum load line impedance.

$$R_o\big|_{N3S0A3} = R_o\big|_{n=3} \tag{2.11}$$

$$R_o\big|_{N3S1A2} = R_{DS_{T2}} + \frac{g_{sd0}+g_{sd1}+g_{m1}}{g_{sd1}\cdot g_{sd0}} \tag{2.12}$$

$$R_o\big|_{N3S2A1} = R_{DS_{T1}} + R_{DS_{T2}} + \frac{1}{g_{sd0}} \tag{2.13}$$

Where $R_{DS}$ is the triode drain-to-source resistance.

In terms of open-loop voltage gain, the hybrid performs similarly to the stacked (Equation 2.7) but the indexer now varies from *i* equals zero to *(a-1)*, as presented in Equation 2.14.

$$A_{vo_n} = \frac{-g_{m0}}{g_{sd0}} \cdot \prod_{i=1}^{a-1}\left(1 + \frac{g_{mi}}{g_{sdi}}\right) \tag{2.14}$$

The voltage distribution of the hybrid follow the two separate rules, which are presented in Algorithm 1. Those guidelines consider an ideal closed switch behavior, so optimization of the voltage distribution is advised.

- for mode $n = a$, voltage distribution follows Equations 2.8, 2.9, and 2.10.
- for modes $n \neq a$, voltage distribution follows Algorithm 1.

**Algorithm 1** Voltage allocation for the hybrid when $n \neq a$ :

**for** $i \in 0 < \mathbb{N} < n$ **do**
  **if** $i < a$ **then**
    $V_{Di} = V_{DS} \cdot (i + 1)$
    $V_{Gi} = V_{GS} + i \cdot V_{DS}$
  **else if** $i \geq a$ **then**
    $V_{Di} = V_{D(i-1)}$
    $V_{Gi} = V_{Di} + 1$
  **end if**
**end for**

Finally, to exemplify how the previous equations and algorithm behave, an ideal voltage allocation for $n$ equals four and $V_{MAX}$ equals two volts is presented in Table 2.1.

**Table 2.1** Example of a possible voltage allocation of a hybrid with $n$ equals four, in volts.

| Modes | $V_{G0}$ | $V_{D0}$ | $V_{G1}$ | $V_{D1}$ | $V_{G2}$ | $V_{D2}$ | $V_{G3}$ | $V_{D3}$ | $V_{DD}$ |
|---|---|---|---|---|---|---|---|---|---|
| N4S0A4 | 0.5 | 1.0 | 1.5 | 2.0 | 2.5 | 3.0 | 3.5 | 4.0 | 4.0 |
| N4S1A3 | 0.5 | 1.0 | 1.5 | 2.0 | 2.5 | 3.0 | 4.0 | 3.0 | 3.0 |
| N4S2A2 | 0.5 | 1.0 | 1.5 | 2.0 | 3.0 | 2.0 | 3.0 | 2.0 | 2.0 |
| N4S3A1 | 0.5 | 1.0 | 2.0 | 1.0 | 2.0 | 1.0 | 2.0 | 1.0 | 1.0 |

## 2.4 STATE-OF-THE-ART OF MULTIMODE PAS

THE efforts present in the literature discussing multimode PAs can be outlined as the combination of different structures and techniques, in which the latter defines the former. Common techniques found in the recent literature are:

- Power cell selection: the process of enabling and/or disabling parallel amplifying cells. Such units are self-contained amplifiers that may be arranged in cascode, stacked, or CS configurations, for example. This technique is employed in Modesto et al. (2019), Ou et al. (2017), and Santos et al. (2016).
- Supply voltage scaling: the increase or decrease of the supply voltage. Modesto et al. (2019) and Kuang et al. (2015) employ this technique.
- Load modulation: the selection of different, pre-defined, optimum output load impedances. May be achieved with a reconfigurable output matching network, for example. Examples of the usage of such technique can be found in Modesto et al. (2019), Ou et al. (2017), and Yin et al. (2014).

- Power combination selection: the process of allowing or not the combination of different sources of power. This technique can be achieved by employing a multiple input single output transformer, for example, and can be found in Luong et al. (2018).
- Body biasing: the process of selecting the voltage applied to the body terminal of a transistor. An example of such usage is present in Hsieh and Tsai (2017).
- Architecture selection: selecting among different and pre-defined architectures for the amplifier. For example, alternating between cascode and stacked arrangements, for example. In Kuang et al. (2015) this technique is discussed.
- Bias selection: setting the bias of the amplifiers so they can operate in different classes. Yin et al. (2014) is an example of such technique being employed.

In Modesto et al. (2019) a multi-propagation path two-stage twelve-mode cascode 130 nm CMOS PA at 2.4 GHz measuring 1.7 $mm^2$ is proposed. Its power stage is composed of three parallel power cells each with a differently sized single-ended cascode structure (Figure 2.6-A). The mechanisms to achieve reconfigurability in this circuit are the combination of on/off states in these power cells, a low pass $\pi$ reconfigurable output matching network to tune the optimum load impedance, and supply voltage scaling (from 1.1 V to 1.8 V). When in high-power mode, EN1, EN2 and EN3 are set to $V_{DD}$ and the output power is the combination of powers delivered by each individual cell. When in low-power mode, EN3 and EN2 are set to 0 V and EN1 to $V_{DD}$, causing only cascode M1-M0 to deliver power to the load. The intermediate efficiency profiles are achieved when different combinations of enabled/disabled cascode cells occur, intermediate $V_{DD}$s are set, and capacitances in the matching network are adjusted (capacitances varies from approximately 500 fF to 1.5 pF). The difference between low and high-power modes is significant: the output referred 1 dB compression point ($OCP_{1dB}$) varies 8.1 dB, the power added efficiency (PAE) at $OCP_{1dB}$ varies 8.8 percentage points (pp), the saturated output power ($p_{sat}$) varies 8 dB and finally peak PAE varies 11.5 pp. A disadvantage of such circuit is the rather complex scheme to select modes.

In Luong et al. (2018) a multi-propagation path two-stage four-mode (dual high power, dual low power) 65 nm CMOS PA at 2.5 GHz measuring 3.2 $mm^2$ is presented. Its power stage is composed of four parallel power cells and each of them is designed with a differential tripple cascode structute (Figure 2.6-B presents a half section of one differential structure). Power selectivity is attained via a mechanism of applying $V_{DD}$ or 0 V to each input's center tap of an integrated four-to-one output transformer: by applying 3 V to the first and last taps and 0 V to the second an third taps, low-power mode is achieved; if 3 V is applied to all four taps, high-power mode is attained. Additionally, low and high efficiency submodes are achieved by changing the biasing of the CS transistors (high or low power, high-efficiency: $V_{BIAS1}$ = 0.55 V and $V_{BIAS2}$ = 0.42 V; high or low power, low-efficiency: $V_{BIAS1}$ = 0.67 V and $V_{BIAS2}$ = 0.20 V). Considering only the modes that have the highest efficiency only and a $p_{out}$ of 20 dBm, the high-power mode performs almost 7 pp higher[1] than the low-power mode. The disadvantages of such configuration are the size of the circuit due to the presence of transformers and modes two and four are not horizontally spaced to modes one and three (respectively) limiting their overall contribution to the circuit in terms of optimized efficiency versus output power.

In Ou et al. (2017) a multi-propagation path two-stage dual-mode 180 nm CMOS PA at 2.4 GHz measuring 2.3 $mm^2$ is described. Its power stage is composed of four parallel power cells with each one designed with cascode structures (Figure 2.6-C). Multimode operation is

[1]Graphically determined.

achieved by changing the output matching network and enabling or disabling such power cells: at high-power mode the input signal is differential and all cells are enabled under same biasing condition, M18 switch is closed and C8 is employed in the output matching. At low-power mode VGH is set 0 V and only cascode M13-M12 operates under VGL biasing. Switch M18 is opened and only C7 participates in the matching (under this condition, input signal is single-ended). Considering its comparative performance in terms of $OCP_{1dB}$, high-power mode is 7.3 dB higher than low-power mode. However, considering a $p_{out}$ of 15 dBm, PAE of low-power mode is almost 2.3 times higher than PAE of the high power.

In its turn, Hsieh and Tsai (2017) presents a single propagation path tri-mode 180 nm CMOS PA operating at 24 GHz measuring 1.3 $mm^2$. Its power stage is composed of a power cell designed with a single-ended three-cascode structure (Figure 2.6-D). Multimode operation is determined by the voltage applied to the body terminal of the CS amplifier (M21). If $V_{BODY}$ equals zero volts, the PA operates under balanced efficiency and linearity regimen (normal mode). If $V_{BODY}$ is equal to 1 V, linearity is improved (linear mode) and if $V_{BODY}$ is equal to -2 V, efficiency is enhanced (efficient mode). At linear mode, this PA's $OCP_{1dB}$ is improved by 8.7 dB in relation to the efficient mode but performs 3.9 pp lower in terms of peak PAE. The disadvantages of such circuit is the need of using the tripple-well transistors and efficiency profiles are not well horizontally spaced.

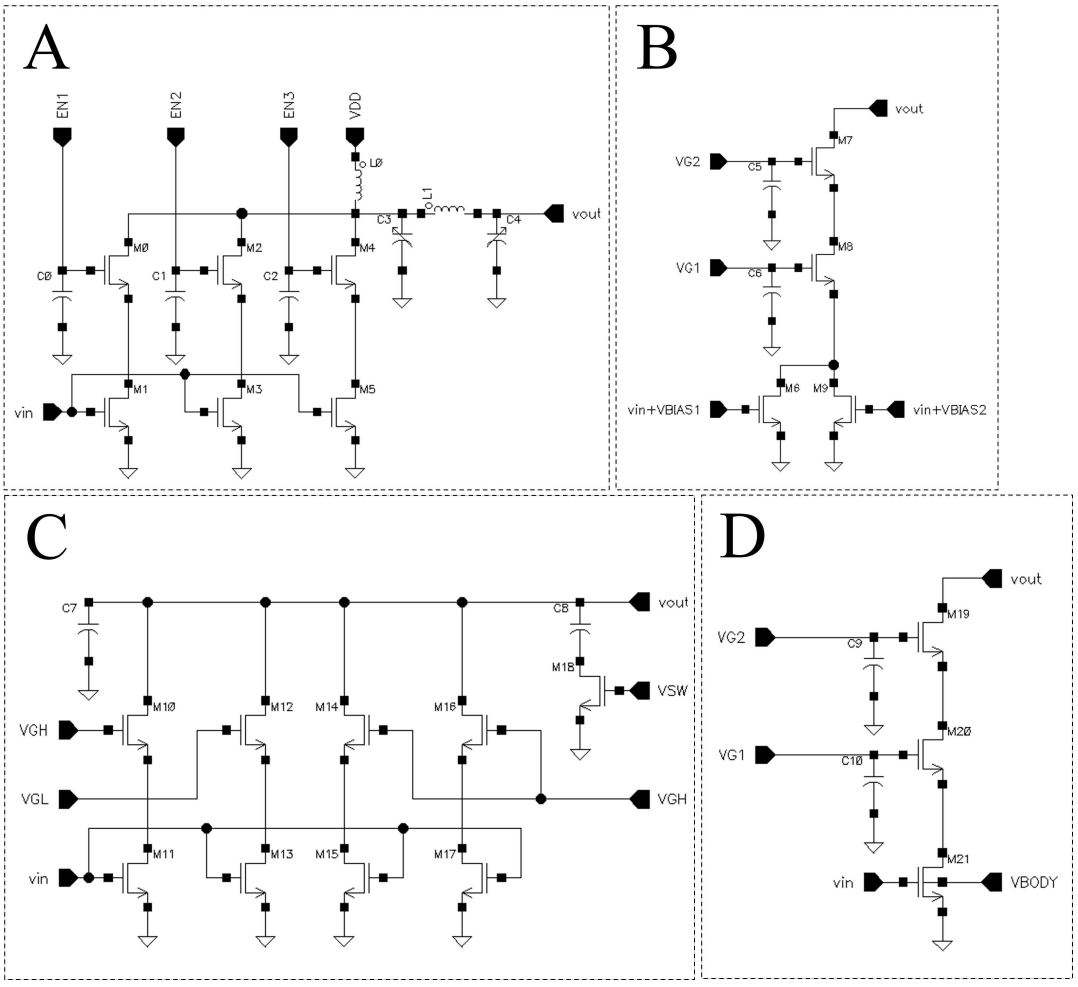


Figure 2.6: Non-exhaustive examples of multimode PAs found in the literature. Adapted from Modesto et al. (2019) (A), Luong et al. (2018) (B), Ou et al. (2017) (C), and Hsieh and Tsai (2017) (D).

It is discussed in Santos et al. (2016) a seven-mode 130 nm CMOS PA operating at 2.4 GHz and measuring 1.7 $mm^2$. Its power stage is composed of three parallel power cells each with a differently sized single-ended cascode structure (Figure 2.7-E). The mechanism to achieve multimode operation is the on/off switching (applying $V_{DD}$ = 1.8 V at the CG or 0 V) of power cells individually. Intermediate efficiency profiles are obtained when different combinations of on/off states are set. The high-power mode of this PA performs an $OCP_{1dB}$ 12.2 dB higher than the low-power mode. However, at a $p_{out}$ of 8 dBm, the low-power mode is 3.4 pp higher than the high-power mode. The disadvantage of this circuit is the proximity of the efficiency profiles at low output powers.

In Kuang et al. (2015) a dual mode 65 nm CMOS PA operating at 60 GHz measuring 0.24 $mm^2$ is presented. Its power stage is composed of a power cell designed with a differential two-stack structure (a single-ended section of the differential power stage is presented in Figure 2.7-F). To achieve dual mode operation, supply voltage is scaled (1.2 V for low power and 2.5 V for high-power modes) and a technique that transforms a two-stacked power cell into a cascode are employed. When VMODE is activated (low-power mode) the pair M29-M30 operate as a cascode amplifier. It so happens because M28 provides a low-impedance path to the ac signal to the gate capacitor C14, which filters out any alternating signal at M29's gate (cascode operation). When VMODE is disabled (high-power mode) R0 and C14 allow voltage swings at the gate of M29 (stacked operation). Operating at 10 dBm $p_{out}$, low-power mode performs a PAE approximately 7 pp higher than high power. However, high-power mode performs almost 8 dB $OCP_{1dB}$ higher than low-power mode.

In the work discussed in Yin et al. (2014) is presented a single propagation path dual-mode 180 nm CMOS PA operating at 2.4 GHz measuring 1.5 $mm^2$. Its power stage is composed of a power cell designed with a differential three-stack structure (Figure 2.7-G) supplied by 5.6 V. Multimode operation is achieved by changing the biasing (VG0) of CS transistor M33 from 0.66 V (low-power mode) to 0.76 V (high-power mode) and by selecting the adequate output matching network ($\pi$ type for low power - L3, C17, and C18 - and L type for high power - L3 and C17) to tune the load impedance. All other voltages in the stack remains unchanged as modes changes. The modes are 5 dB apart in terms of $OCP_{1dB}$ and 4.3 pp in terms of PAE at $OCP_{1dB}$.

A final remark must be made concerning the work presented in Woo et al. (2014). Despite not directly addressing the multimode theme, the work deals with dynamically controlling a quadruple-cascode with similar mechanisms that are proposed in this thesis. In Woo et al. (2014) is presented a single propagation path dynamic controlled quadruple-cascode for envelope tracking 320 nm silicon-on-insulator CMOS PA operating at 837 MHz and measuring 1.05 $mm^2$ (Figure 2.7-H). Such control bases itself on two main mechanisms: increasing or decreasing the supply voltage (which varies from 1 V to 3.4 V) as the envelope amplitude ($V_{ENV}$, which varies from 0 V to 1 V) increases or decreases and adjusting the value of gate capacitances of the CGs. By adequately adjusting these two factors, the structure can behave either as a quadruple-cascode, as a triple-cascode plus a bypassed transistor, and as a cascode plus two bypassed transistors. In a similar way, every time the circuit changes, different efficiency profiles occur. In this sense, the selection of modes ensues when the $V_{ENV}$ is compared to two undisclosed reference voltages ($ref_4$ and $ref_3$, in which the former is greater than the latter). When $V_{ENV}$ is at its maximum, the outputs of two Schmitt trigger comparators (EN3 and EN2) enable S0, S1, and S2 and the four-cascode operation occurs. When $V_{ENV}$ is between $ref_4$ and $ref_3$, the circuit behaves as a triple-cascode by disabling S0. Finally, when $V_{ENV}$ is below $ref_3$, cascode operation is set and S1 and S2 are disabled. The measured circuit is capable of a peak PAE of 64% under quadruple-cascode and 40% under cascode operations. Additionally, this circuit is capable of achieving almost 33 dB gain under qradruple-cascode and 26 dB when operating as a cascode.

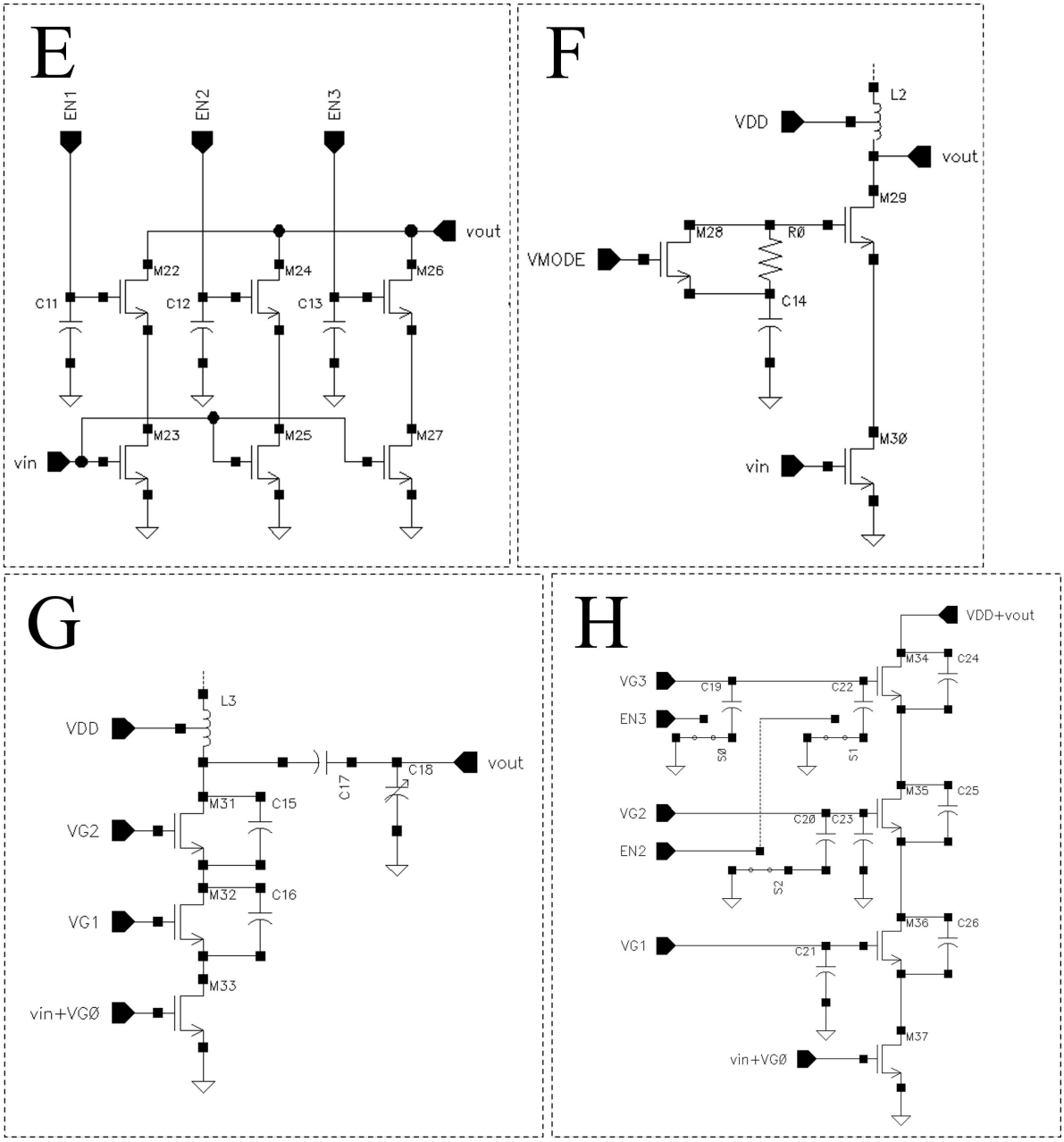


Figure 2.7: Other non-exhaustive examples of multimode PAs found in the literature. Adapted from Santos et al. (2016) (E), Kuang et al. (2015) (F), Yin et al. (2014) (G), and Woo et al. (2014) (H).

A summary of the comparison of the state-of-the-art is presented in Table 2.2.

**Table 2.2** Summary of the main characteristics of the state-of-the-art.

| Reference | Structure | Technique | Area ($mm^2$) | Frequency (GHz) |
|---|---|---|---|---|
| Modesto et al. (2019) | three parallel power cells with differently sized single-ended cascodes | power cell selection, supply voltage scaling, load modulation | 1.7 | 2.4 |
| Luong et al. (2018) | four parallel power cells with differential cascodes | power combination selection | 3.2 | 2.5 |
| Ou et al. (2017) | four parallel power cells with single-ended cascodes | power cell selection, load modulation | 2.3 | 2.4 |
| Hsieh and Tsai (2017) | a power cell with single-ended three-stack | body biasing | 1.3 | 24 |
| Santos et al. (2016) | three parallel power cells with differently sized single-ended cascodes | power cell selection | 1.7 | 2.4 |
| Kuang et al. (2015) | a power cell with differential two-stack | architecture selection, supply voltage scaling | 0.24 | 60 |
| Yin et al. (2014) | a power cell with differential three-stack | bias selection, load modulation | 1.5 | 2.4 |

## 2.5 CONCLUSION

This chapter discussed the theoretical background of the CS, cascode, stacked and a multimode version of it, hybrid, architectures. Stacking is an useful technique which allows the feasibility of high $p_{out}$ PAs in scaled CMOS processes because the strain of a high supply voltage can be distributed among each and every device of the structure. The voltage distribution guidelines for the stacked and hybrid architectures follow a common branch, much as some customization must be considered for the second. This stems from the fact that transistors in this multimode version can behave either as amplifiers or as closed switches. Additionally, it also discussed several power stage structures and techniques to achieve multimode operation in both single and multi-propagation path PA architectures. Regarding the structures, in general, the power stage can be composed of one or more power cells; the power cells may be differential or not and may be in cascode or stacked configurations. In regards to the techniques, they may or may not be the combination of switching on/off of power cells, supply or biasing voltages scaling, load modulation via output matching network reconfigurability, body biasing, and circuit architeture reconfigurability.

In the following chapter, the design of a proof-of-concept hybrid CMOS PA will be presented.

# 3 MULTIMODE PA DESIGN

This chapter will present the schematics and layout of the proof-of-concept based on the hybrid architecture (Section 2.3) and developed to test the hypothesis proposed in Section 1.2. The employed software tools were Cadence Virtuoso (schematic, layout, and simulation environments) version 6.1.8, Cadence Spectre Simulator version 19.1, and Cadence Physical Verification System version 19.1. All necessary verification were dully checked to ensure this circuit could be manufactured, meaning that Design Rule Check (DRC), orthogonality, and Layout Versus Schematic (LVS) were all green passes and the GDS file was created.

## 3.1 CIRCUIT'S OVERVIEW

The block diagram of the proposed circuit is presented in Figure 3.1, which presents six blocks and five pins. The blocks are the input matching network (IMN), the feedback resistor, a capacitor bank, a choke inductor, a power core, and an output matching network (OMN). As for the pins, they are the RF input and output, the supply voltage and the ground, the biasing tree, and the enable pins. The IMN is connected between the RF input and the power core. The OMN, is connected between the power core and the RF output. It is via the choke inductor that the supply voltage is fed to the power core. The feedback resistor is connected between the output of the choke inductor and the output of the IMN. The capacitor bank is connected to the power core and to the enable pins. The IMN, OMN, power core, and capacitor bank are connected to the ground (the substrate of the process). The blue lines in the figure aid to evince the RF signal propagation path of circuit and, as shown, it has no switches or any form of relaying to achieve multimode operation. The enable pins are composed of three distinct pins (LPEN, MPEN, and HPEN) which control mode selection. Lastly, the biasing tree is composed of four distinct pins (VB1, VB2, VB3, and VB4), one for each stacked transistor in the power core.

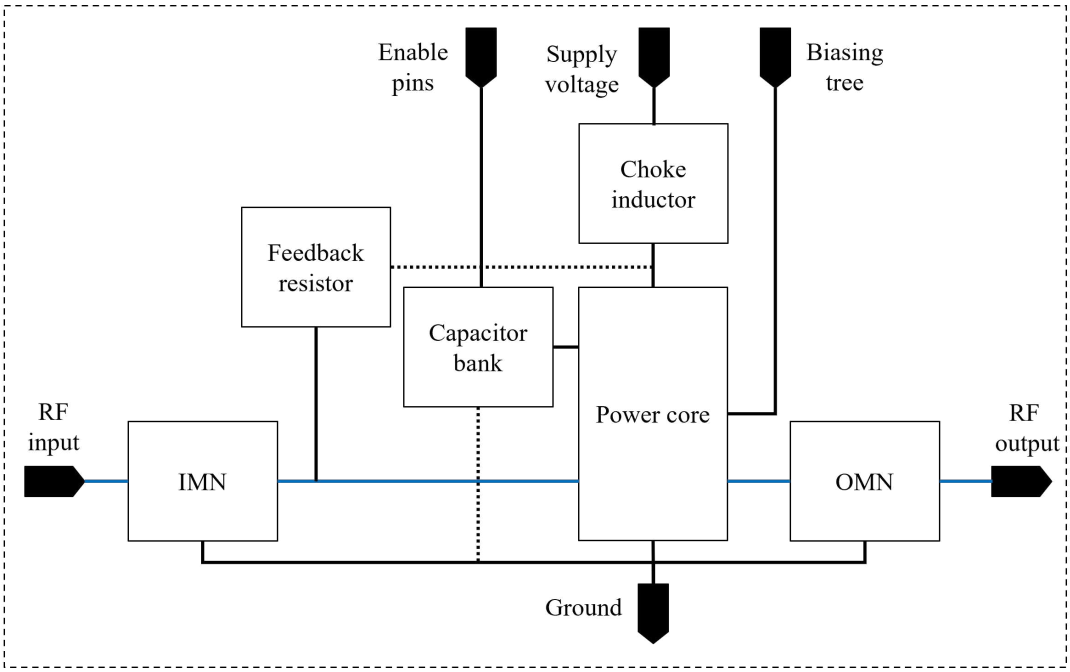


Figure 3.1: Block diagram of the proposed circuit.

## 3.2 SCHEMATIC

The schematic of the proposed proof-of-concept is presented in Figure 3.2. The stack height of four (transistors M0 to M3) in the power core was selected due to three factors: it allows the use of a high supply voltage, and thus, has a high output power capability (for this project, it was expected a linear $p_{out}$ of at least 20 dBm with ideal components); four is a stack height that does not add significant total phase rotation at the drain of M3 (Montaseri et al., 2018), meaning that the core's output power is close to the theoretical output power; and, lastly, four transistors allow four different power modes in the proposed arrangement.

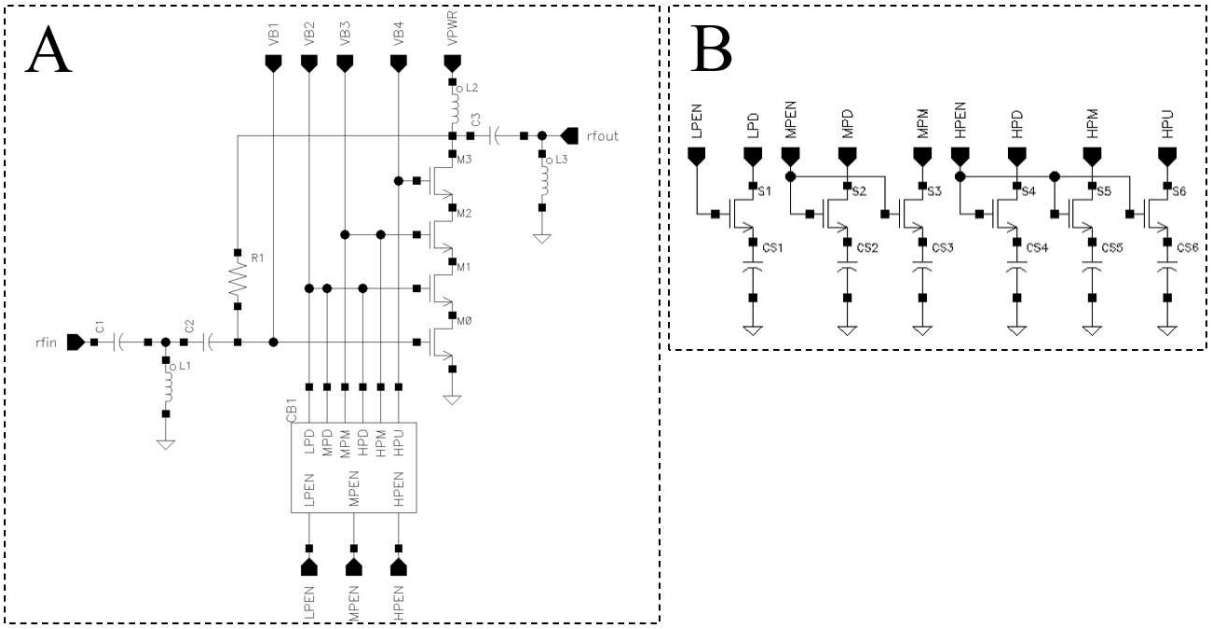


Figure 3.2: Schematic of the proof-of-concept. Inset A presents the PA's circuit while inset B details the capacitor bank CB1.

Regarding the transistor sizing process for M0-M3, this work employed a supervised optimization method based on large-signal targets. The obtained results of such optimization method are: M0-M3: total width of 1.2 mm (60 µm per finger), channel length of 240 nm, 20 fingers, and double multiplicity. This method consists of preparing a test bench in which the number of fingers, the width of a single finger, and multiplicity are considered degrees of freedom and interactively altered. By allowing an adequate range of variation of such values and by specifying targets related to the gain, power, efficiency, and linearity, it was possible to determine adequate sizing of transistors - a flowchart example is presented in Figure 3.3. In Cadence Virtuoso, if it is desired to optimize the number of fingers (nf) of a transistor, its parameter "number of fingers" should be set to "nf" in the schematic view. Under the simulation view, the "nf" value will automatically considered as a design variable and its range of variation can be set varying from zero to ten with step size of one, for example. Then, in the "Outputs setup" tab, expressions (such as $OCP_{1dB}$, for example) are added and the aimed target (field "spec") of 20 dBm can be set. After setting the simulator into optimization mode (such as "Local Optimization"), the simulations are ran and outputs interactively presented to the designer until the target is achieved or optimized. The exemplified process explains the optimization for just one variable, but during circuit development, many variables should be supervised as most of the time not all targets are achievable and the designer should consider the trade-offs of the design. This is a versatile and helpful method in which its benefits stem from presenting the outputs to the

designer as soon as the simulations are ran, reducing overall setup-time, and allowing an efficient comparison between previous simulation results. It differs from the typical "variable sweeping" method as the optimization method bases itself on built-in algorithms that keep track of the causes and effects of variations - the simulator registers when to stop to increase or decrease a parameter if its contribution to the target is minimal. On the other hand, it also makes the complexities of PA design transparent, which is not advisable for new designers.

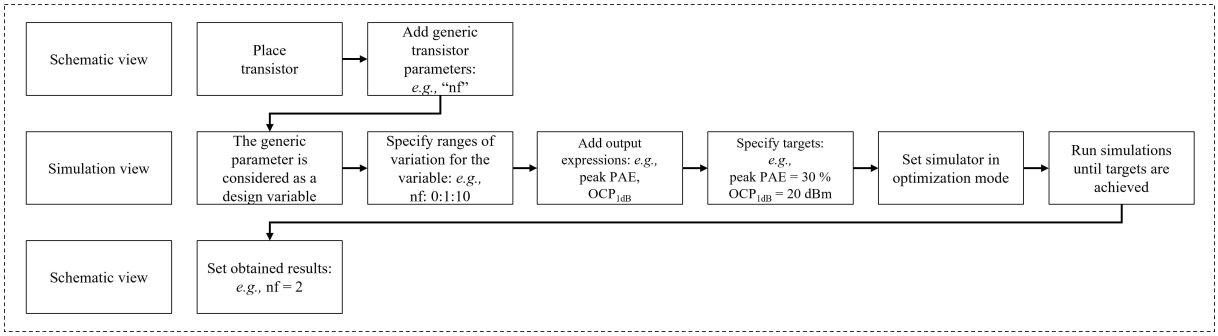


Figure 3.3: Flowchart example of the optimization process for the amplification core sizing.

Regarding the sizing of the switches S1 to S6 in the capacitor bank CB1 of Figure 3.2-B, a similar optimization process was conducted with the characteristics of interest now being small-signal ones, such as drain-to-source capacitance ($C_{ds}$) and $R_{DS}$. The outcome of such optimization process was: S1-S6: total width of 200 µm (10 µm per finger), channel length of 240 nm, 20 fingers, multiplicity of one, $C_{ds}$ of 50.8 fF, and $R_{DS}$ of 5.25 Ω.

The biasing and supply voltages are fed through VB1 to VB4 and VPWR of Figure 3.2, respectively. The biasing voltages are fed trough external voltage sources, which, consecutively, are connected directly to the gates of the transistors in the power core. These external voltage sources should be connected to the circuit via RF chokes so no ac gate voltage is shorted to the ground through them. The capacitor bank CB1 (Figure 3.2-B) is also connected to the gates of the power core. When the mode is selected, different combinations of capacitances (CS1 through CS6) are connected or not to the gates of the stack, limiting the peak differential voltages from reaching the technology maximum rated voltage levels.

The IMN, which is composed of C1, C2, and L1, employs a conjugated-match high-pass T network that matches 50 Ω to the average input impedance of each mode ($\overline{Z_{in}}$) at 2.4 GHz (7.29-j84.9 Ω) - this highlights another interesting aspect of the proposed PA: as modes changes, $Z_{in}$ varies little (standard deviation for all modes is 0.32-j1.72 Ω) resulting in almost overlapping input impedance scattering curves (as will be discussed in chapter 4, Figure 4.7).

The choke inductor (L2) at 2.4 GHz is an important passive which both blocks the RF swings at the drain of M3 to be fed into the supply voltage and, together with C3 and L3, participates in the output matching.

The OMN (C3 and L3), in its turn, employs a power-match high-pass L network matched from the PA's selected load-pull impedance ($Z_{loadpull}$) at 2.4 GHz of 37+j22 Ω to 50 Ω. As show in Figure 3.4, which presents the loadpull simulation regarding $OCP_{1dB}$ and PAE, such selected $Z_{loadpull}$ is an adequate compromise for all modes in terms of efficiency and linearity, while still maintaining the transistors below $V_{MAX}$ voltage.

Both IMN and OMN were designed with an impedance matching network designer[2] which provided the ideal passive values for the circuits. Both configurations were selected among

[2]Available at https://home.sandiego.edu/ ekim/e194rfs01/jwmatcher/matcher2.html

others because they presented the lowest component count. During layout, these values should be adjusted due to parasitic impedances.

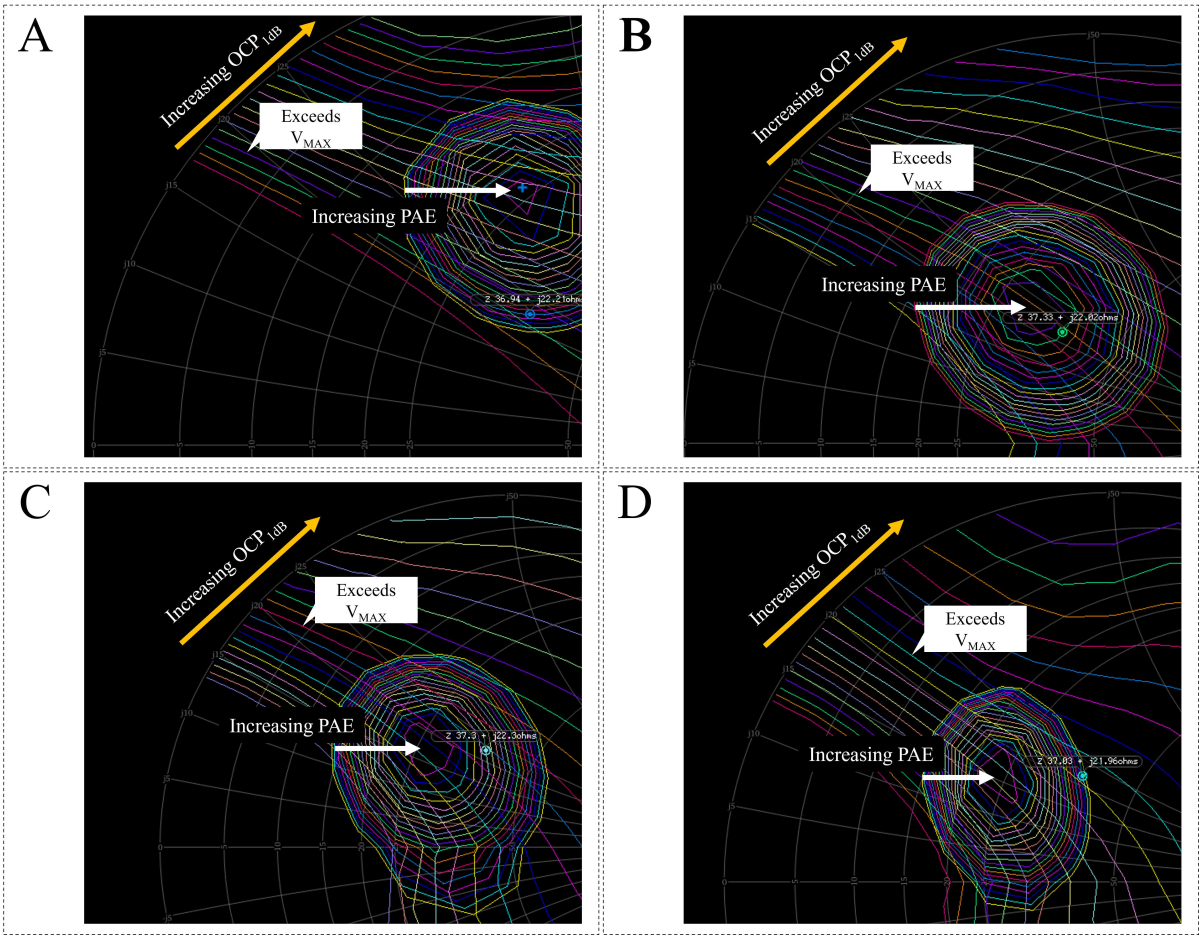


Figure 3.4: $OCP_{1dB}$ (open curves) and PAE (closed contours) results from load pull impedance analysis for all four modes at 2.4 GHz. In each figure, the approximate 37+j22 Ω impedance is show. Inset A: N4S3A1, inset B: N4S2A2, inset C: N4S1A3, inset D: N4S0A4.

This circuit has four distinct efficiency profiles: N4S3A1, N4S2A2, N4S1A3, and N4S0A4 modes. The selection of modes is achieved by maintaining VB1 fixed to 0.52 V (a class A biasing point for the CS) in the biasing tree while changing the voltages VB2, VB3 and VB4. In this sense, at N4S0A4 mode VB2, VB3 and VB4 are set to 2.0 V, 2.4 V, and 3.6 V. At N4S1A3 VB2, VB3 and VB4 are set to 2.0, 2.4 V and 4.8 V, respectively. At N4S2A2, VB2 equals 2.0 V, and VB3 and VB4 are equal to 4.8 V. Finally, for N4S3A1 operation, VB2, VB3, and VB4 are all set to 4.8 V. Additionally to setting the proper voltage to the biasing tree, two additional steps are used to optimize circuit operation: step 1, enable the proper capacitor bank and step 2, set the supply voltage. Regarding step 1, if N4S0A4 mode is intended, HPEN pin should be exclusively enabled with 4 V (other enable pins must be grounded). The same logic applies to the enabling/disabling of the remaining modes, except for N4S3A1, which all enable pins are grounded. Regarding to the step 2, supply voltage (VPWR) should be set to 3.8 V in N4S0A4 operation, 3.2 V at N4S1A3 mode, 2.6 V at N4S2A2 mode, and 2.0 V at N4S3A1. In Table 3.1 is summarized the PA operation mode set-up.

**Table 3.1** Summary of the set-up of all four efficiency profiles.

| Mode | Biasing tree (V)<br>VB1, VB2, VB3, VB4 | Enable pins (V)<br>LPEN, MPEN, HPEN | Supply<br>voltage (V) |
|---|---|---|---|
| N4S3A1 | 0.52, 4.8, 4.8, 4.8 | 0, 0, 0 | 2.0 |
| N4S2A2 | 0.52, 2.0, 4.8, 4.8 | 4, 0, 0 | 2.6 |
| N4S1A3 | 0.52, 2.0, 2.4, 4.8 | 0, 4, 0 | 3.2 |
| N4S0A4 | 0.52, 2.0, 2.4, 3.6 | 0, 0, 4 | 3.8 |

A summary of the passive's values is: C1: 303.46 fF; C2: 900 fF; C3: 1.9 pF; CS1: 1 pF; CS2: 1.3 pF; CS3: 1 pF; CS4: 2.9 pF; CS5: 2 pF; CS6: 800.0 fF; L1: 4.25 nH; L2: 1.8 nH; L3: 5.49 nH; R1: 3.44 kΩ and a summary of the schematic-level dc operating points of FETs M0-M3 for each mode is presented in Table 3.2. Additionally, it also presents the comparison between calculated and simulated values of $R_o$ and $A_{vo}$ for all modes. For the calculated values, equations 2.11, 2.12, 2.13, 2.6, and 2.14 were employed. The simulated values were obtained from a test bench in which only transistors were present.

**Table 3.2** Summary of the schematic-level dc operating points.

| Mode | $I_D$ (mA) | $V_{GS}$ (V)<br>M0, M1, M2, M3 | $V_{DS}$ (V)<br>M0, M1, M2, M3 | $g_m$ (S)<br>M0, M1, M2, M3 | $g_{ds}$ (S)<br>M0, M1, M2, M3 | $V_{TH}$ (V)<br>M0, M1, M2, M3 | Calculated Ro (Ω) | Simulated Ro (Ω) | Calculated $A_{vo}$ (V/V) | Simulated $A_{vo}$ (V/V) |
|---|---|---|---|---|---|---|---|---|---|---|
| N4S3A1 | 17.2 | 520.0 m, 2.8,<br>2.8, 2.8 | 2.0, 5.5 m,<br>5.5 m, 5.5 m | 240.6 m, 2.5 m,<br>2.5 m, 2.5 m | 9.4 m, 3.1,<br>3.1, 3.1 | 413.3 m, 479.6 m,<br>479.6 m, 479.6 m | 107 | 107 | 25.5 | 25.5 |
| N4S2A2 | 12.8 | 520.0 m, 533.8 m,<br>2.2, 2.2 | 1.5, 1.1,<br>4.6 m, 4.6 m | 196.5 m, 194.6 m,<br>122.8 m, 124.3 m | 1.5, 1.1,<br>4.6 m, 4.6 m | 431.5 m, 443.4 m,<br>479.6 m, 479.6 m | 3.4 k | 3.4 k | 637.0 | 638.4 |
| N4S1A3 | 12.5 | 520.0 m, 563.1 m,<br>524.7 m, 1.6 | 1.4, 438.3 m,<br>1.32, 5.8 m | 194.1 m, 185.2 m,<br>193.5 m, 7.7 m | 7.7 m, 9.3 m,<br>7.8 m, 2.1 | 432.5 m, 467.4 m,<br>436.6 m, 479.6 m | 72.7 k | 73.0 k | 13.6 k | 13.6 k |
| N4S0A4 | 12.5 | 520.0 m, 563.3 m,<br>503.3 m, 548.5 m | 1.4, 433 m,<br>1.3, 749.0 m | 194.1 m, 185.0 m,<br>192.6 m, 189.3 m | 7.7 m, 9.4 m,<br>7.9 m, 8.3 m | 432.5 m, 467.5 m,<br>441.4 m, 456.6 m | 1.69 M | 1.69 M | 315.4 k | 303.5 k |

## 3.3 LAYOUT

The circuit was designed with the GlobalFoundries 130 nm 8HP CMOS RF process, which, in its turn, is based on IBM's 130 nm 8SF CMOS RF process (Candra et al., 2013). The employed version of the technology has seven metalization layers (with thin and thick metals), integrated passives (resistors, capacitors, and inductors), and thin, thick, triple-well and RF versions of planar FETs.

The layout measuring 813 µm by 493 µm (without pads) of the schematic in Figure 3.2 is presented in Figure 3.5 and each major block of section 3.2 is delimited. The circuit was mostly routed with thick top level metals as they have low parasitic resistance and capacitance. Low level metals were only used to access transistor's terminals or inductors' shields. After the circuit was laid out, RC parasitics were extracted and post-layout simulations were performed.

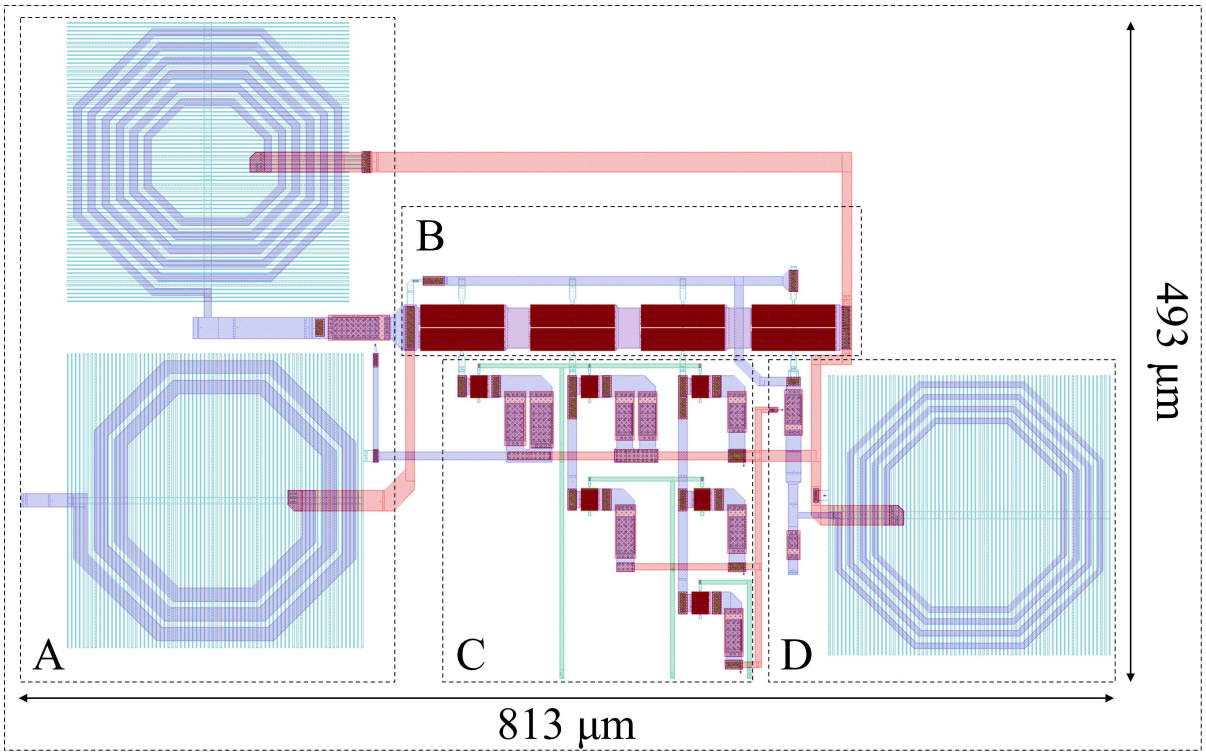


Figure 3.5: Layout of the proposed proof-of-concept measuring 813 µm by 493 µm. Inset A - OMN (upper portion) and choke inductor, inset B - amplification core and feedback resistor, inset C - capacitor bank, and inset D - IMN.

Regarding the process of laying out the circuit, an accumulative cyclic approach was employed. This method is cyclic because it is based on laying out each individual block of the circuit, running design verification (design rule checks - DRC - orthoganality checks, and, layout-versus-schematic - LVS - checks), extracting RC parasitics, simulating the circuit, comparing obtained post-layout and schematic results, and repeating as necessary. By doing so, it is easier to determine which sections of the layout has problems and should be improved; it is accumulative because after being verified, the individual block is fixed and a new one is laid out following the same cycle. When all blocks are ready, the consolidated version is one last time verified, extracted, and simulated.

It is normal during this process to observe drastic differences on the some characteristics of the PA: some may be degraded and some may be improved. For example: during schematic-level simulations, the obtained $\overline{Z_{in}}$ was 9.1 - j81.48 Ω with a zero standard deviation. Input matching ($S_{11}$) at 2.4 GHz had a performance below -20 dB. In this sense, it depends on the experience of the designer to act or not when faced with such differences.

In regards to the employed cells, R1, is an unsilicided over-isolation p-type polysilicon resistor. Among all available cells, it has the highest sheet resistance and sheet resistance tolerance but the lowest resistance variation with temperature and a null voltage coefficient. Apart from that, it has low parasitic capacitance and no latch-up effect, as this passive does not include a parasitic diode junction - such characteristics make this cell the best option for the feedback resistor R1.

As for the capacitors (C1-C3 and CS1-CS6), the single Metal-Insulator-Metal (MIM) capacitors were selected. They are formed by two metal layers separated by an nitride insulator. Although this configuration has three times lower capacitance per area than the dual version, it benefits of a lower capacitance dependence with temperature and is well suited for the capacitance range of the selected application.

Regarding the inductors (L1, L2, and L3), although the process allows three different types of cells for single ended applications, the wiring option available for the employed version has only one: the planar spiral inductor. This option has low equivalent series resistance, high quality factor, and lowest parasitic capacitance among all options at cost of a lower overall peak quality factor. Interestingly, the inductor's spiral is formed in the same metalization level of the bottom plate of the single MIM capacitor, but its structure has a low level metal grate that is employed to shield (light-blue parallel lines in the inductors of Figure 3.5) the structure from substrate noise and to prevent induced currents in the substrate at cost of increased parasitic capacitance.

Finally, for the active devices, the employed cells were the thick oxide n-channel field effect transistor with guard-ring. This version of the typical n-channel FET has its gate oxide thickness and channel length approximately 2.3 and two times larger, respectively. Differently from the non-RF version, this device has controlled geometry which allows an accurate electrical simulation.

## 3.4 CONCLUSION

This chapter discussed the schematic and layout for the developed proof-of-concept. In regards to the schematic, it is composed of a hybrid core with $n$ equals four, which, in its turn, determines four efficiency profiles. Besides selecting the supply voltage and bias of each transistor, a capacitor bank allows the selection of the appropriate capacitance at each gate of the structure. For the layout, it was designed used the native passives of the employed CMOS process. The layout area of proof-of-concept measures 0.4 $mm^2$ (does not include pads) and verification (DRC, orthogonality, and LVS) were dully checked before resistance and capacitance parasitics were extracted.

The following chapter will present and discuss the obtained post-layout simulation results.

# 4 VALIDATION

THIS chapter will deal with the presentation and discussion of the obtained post-layout simulation results for the circuit discussed in Chapter 3 under the operation condition presented in Table 3.2 and after resistance and capacitace parasitics extraction. The employed metrics to characterize the proposed PA are separated in three classes: continuous-wave small and large-signal, and modulated sources.

Examples of the small-signal metrics are the scattering parameters. As for the large-sinal metrics, gain, linearity and efficiency, described by gain, $OCP_{1dB}$, and PAE were employed. As for the metrics for modulated sources, Error Vector Magnitude (EVM) and Adjacent Channel Power Ratio (ACPR) were considered.

Besides those simulations, a large-signal operation under extreme conditions was conducted via the Process Voltage Temperature (PVT) analysis.

Lastly, although this architecture allows four-mode operation, the project requirement was a three-mode PA. the four-stack architecture was employed because it allowed using a high supply voltage, which, in turn, allowed the structure to achieve more than 20 dBm $OCP_{1dB}$ (under schematic simulations) - in fact, the post-layout three-mode operation PA was presented in Santos et al. (2020). In this sense, modes N4S2A2, N4S1A3, and N4S0A4 were object of preferred optimization and enhancement, which, in turn, caused mode N4S3A1's continuous-wave results to be shadowed by the other modes. Apart from this characteristic and considering completeness, this thesis will present and discuss all attainable modes of this architecture simulated with 50 Ω source and load resistances.

## 4.1 CONTINUOUS-WAVE SMALL AND LARGE-SIGNALS RESULTS

In terms of power performance, Figure 4.1 presents the Gain versus $p_{out}$ curves for the four efficiency profiles at 2.4 GHz. Under small-signal operation the power gain is 5.6 dB, 8.2 dB, 9.6 dB, and 8.8 dB for N4S3A1, N4S2A2, N4S1A3, and N4S0A4 modes, respectively. Based on Equation 2.7, one may infer a higher gain of N4S0A4 in comparison to N4S1A3. This situation, however, was not translated into the proposed circuit due to the influence of the feedback resistance in the amplification core: as R1 is connected from the drain of M3 to the gate of M0 and as the proposed circuit is single-propagation path multimode PA, varying R1 translates into non-uniform variation of stability, linearity, efficiency, and gain across all modes. Thus, the selected value of R1 was a compromise that translated into an overall stable circuit, but which also meant the reduction of the gain of N4S0A4. Lastly, the PA achieves $OCP_{1dB}$ of 15.2 dBm, 16.8 dBm, 18.1 dBm, and 19.9 dBm for the N4S3A1, N4S2A2, N4S1A3, and N4S0A4 modes.

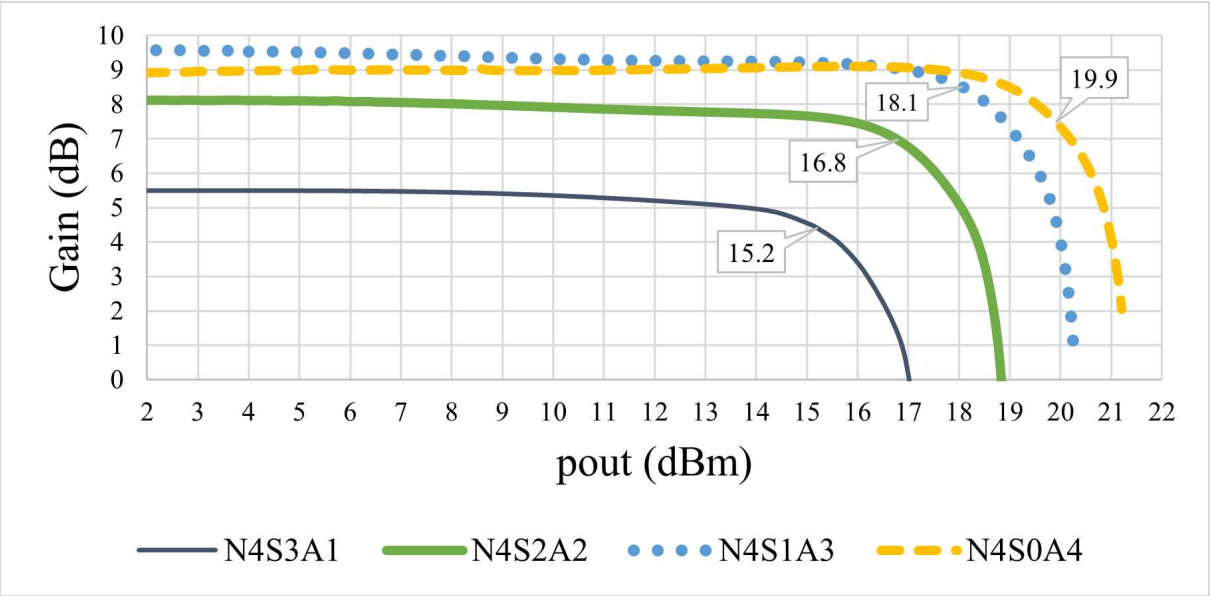


Figure 4.1: Power gain as function of $p_{out}$ for all four modes at 2.4 GHz. The boxes in each curve present the $OCP_{1dB}$ of each mode.

In Figure 4.2 the curves of PAE in function of $p_{out}$ are presented for the four efficiency profiles at 2.4 GHz. At $OCP_{1dB}$, the PA achieves a PAE of 20.5% at N4S3A1, 28.1% at N4S2A2, 28.9% at N4S1A3, and 25.7% at N4S0A4. At peak PAE, the PA performs 20.5%, 28.1%, 28.9%, and 25.7% for modes N4S3A1, N4S2A2, N4S1A3, and N4S0A4, respectively. The comparison of Figure 4.2 and Figure 4.3 provides an insight on how important is the selection of adequate gate capacitances. Observe that mode N4S0A4 under a $V_{DD}$ of 3.2 V is almost 8 pp lower than mode N4S1A3, which is supplied by 3.2 V but has the adequate gate capacitance set. The explanation of this phenomenon can be found in the work Jeong et al. (2009): when $V_{DD}$ is scaled down, the drain voltage of the transistors move from saturation to triode region. As this happens, the capacitances at the drains of the stacked transistors increase significantly, unmatching the output impedance of the stack to the selected $Z_{loadpull}$. As gate capacitors directly affect on the impedances (see Section 2.2), they are employed to compensate such behavior.

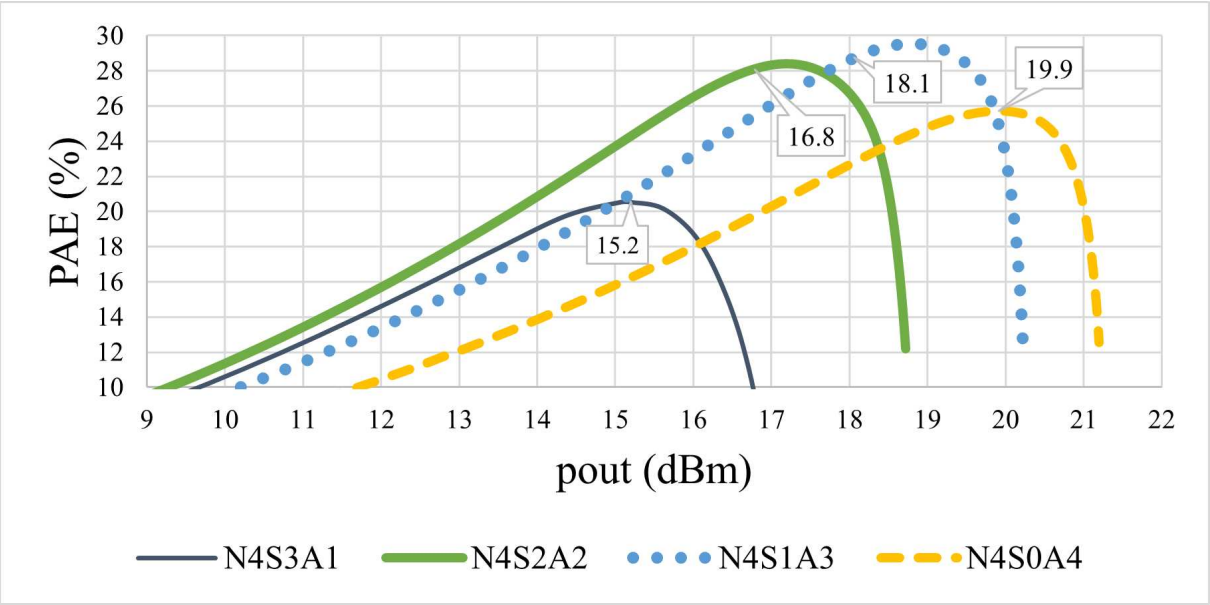


Figure 4.2: PAE as function of $p_{out}$ for all modes at 2.4 GHz. The boxes in each curve present the $OCP_{1dB}$ of each mode.

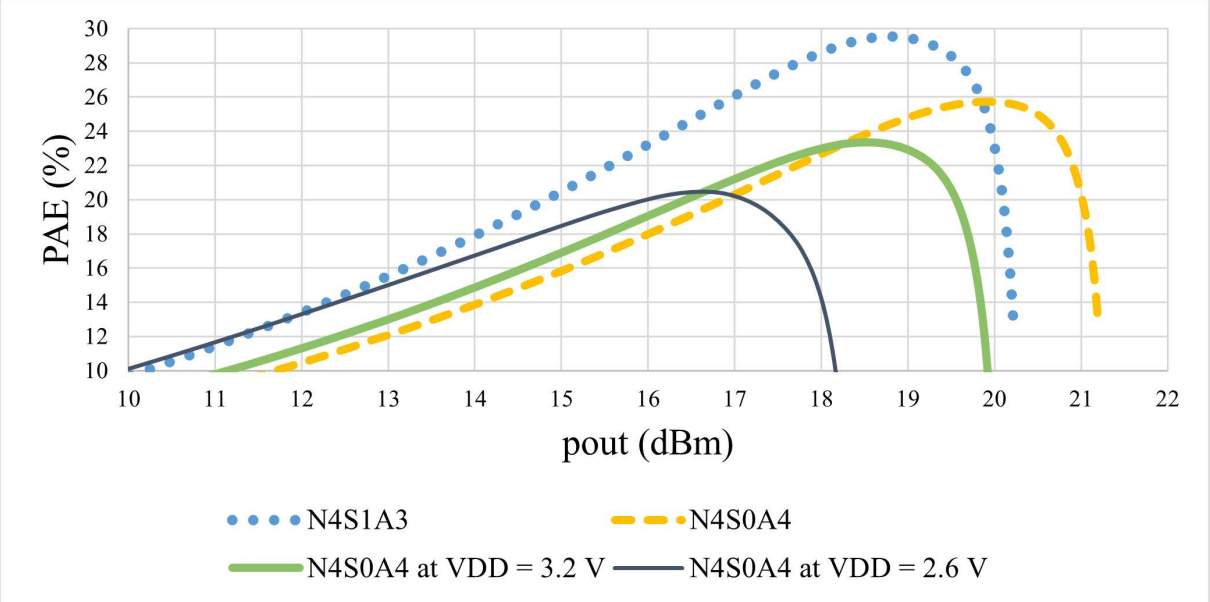


Figure 4.3: PAE as function of $p_{out}$ for N4S0A4 at 2.4 GHz at $V_{DD}$ equals 2.6 V and 3.8 V.

Considering $p_{peakPAE}$, which is the output power when maximum efficiency occurs, the multimode device achieves 15.1 dBm, 17.2 dBm, 18.8 dBm and 19.9 dBm, for N4S3A1, N4S2A2, N4S1A3, and N4S0A4 modes. The differences between $p_{peakPAE}$ and $OCP_{1dB}$ are: 0 dB, 0.4 dB, 0.7 dB, and 0 dB, which renders to a PA optimized to linear operation. Considering power control range regarding $OCP_{1dB}$, the presented PA has a total range of 4.8 dB for all modes. N4S3A1 and N4S2A2 modes are 1.7 dB apart, N4S2A2 and N4S1A3 modes are 1.3 dB apart and N4S1A3 and N4S0A4 modes are 1.8 dB apart.

In terms of power control range as a function of efficiency, N4S2A2 has the highest PAE up until 17.7 dBm. From $p_{out}$s of 17.7 dBm to 19.9 dBm, N4S1A3 has the highest PAE. From a $p_{out}$ of 19.9 dBm and onward, N4S0A4 achieves highest overall efficiencies. N4S3A1

operation has efficiency higher than N4S1A3 and N4S0A4 up until 15 dBm, approximately, but never higher than N4S2A2's efficiency. The presented power ranges consider the best operation in terms of $p_{out}$ and efficiency and, thus, the interface output powers of 17.7 dBm and 19.9 dBm should be considered as the triggers for mode-switching under continuous-wave operation.

Considering only a single-tone 2.4 GHz signal, N4S3A1 mode has no advantage over other modes; its efficiency, linearity, and gain are always lower than those of other modes. As mentioned earlier in chapter 1, efficiency profiles should somehow be horizontally spaced so the PA could benefit from an efficiency-optimized power control range: this is the case for modes N4S2A2, N4S1A3, and N4S0A4 but not for N4S3A1. This mode is shadowed by N4S2A2 characteristics, rendering it unsuited for an operation under a continuous-wave, single-tone, 2.4 GHz signal. A summary of the presented power characteristics for the proof-of-concept is presented in Table 4.1.

**Table 4.1** Summary of the power performances at 2.4 GHz for all modes.

| Mode | Gain (dB) | $OCP_{1dB}$ (dBm) | PAE at $OCP_{1dB}$ (%) | $p_{peakPAE}$ (dBm) | peak PAE (%) |
|---|---|---|---|---|---|
| N4S3A1 | 5.6 | 15.1 | 20.5 | 15.2 | 20.5 [1] |
| N4S2A2 | 8.2 | 16.8 | 28.1 | 17.2 | 28.4 |
| N4S1A3 | 9.6 | 18.1 | 28.9 | 18.8 | 29.5 |
| N4S0A4 | 8.8 | 19.9 | 25.7 | 19.9 | 25.7 [1] |

[1]Efficiency at $p_{peakPAE}$ is less than 0.1 percentage points apart from efficiency at $OCP_{1dB}$.

As for the linearity in function of frequency, Figure 4.4 presents the $OCP_{1dB}$ from 1.2 GHz to 4 GHz curves for all modes. From 2.2 GHz to 2.6 GHz, N4S3A1 maintains $OCP_{1dB}$ over 13.6 dBm, N4S2A2 over 15.3 dBm, N4S1A3 over 16.9 dBm, and N4S0A4 over 18.8 dBm. Regarding efficiency, it is presented in Figure 4.5 the PAE at $OCP_{1dB}$ versus frequency curves for all four modes. From 2 GHz to 3 GHz, N4S3A1 maintains efficiency over 8.3%, N4S2A2 over 12.8%, N4S1A3 over 12.4%, and N4S0A4 13.2%.

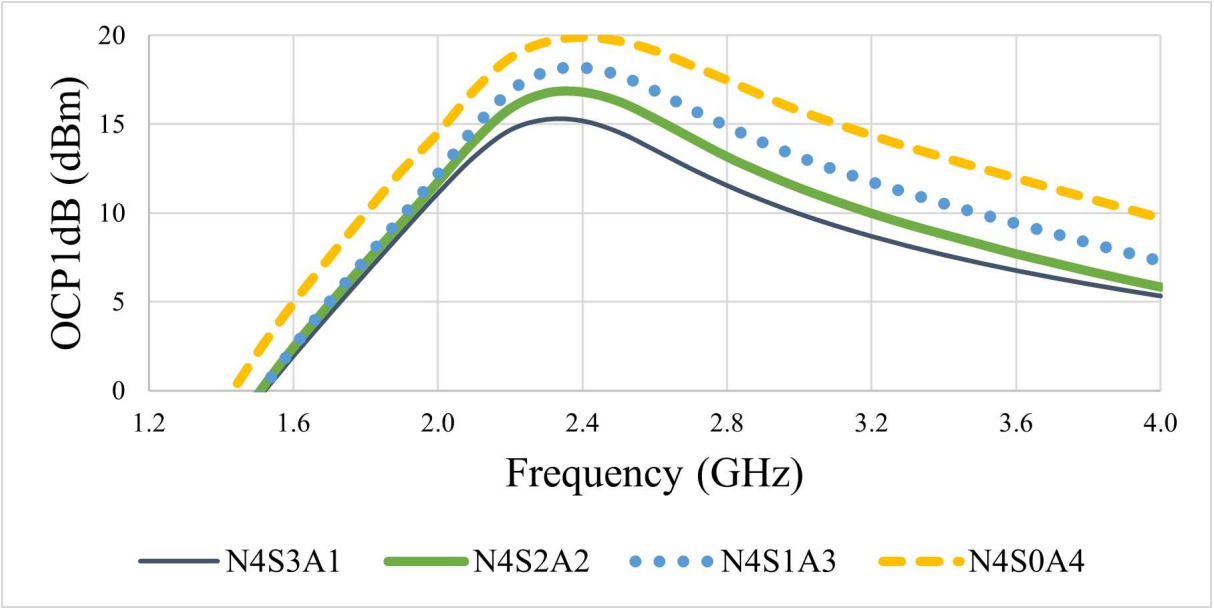


Figure 4.4: $OCP_{1dB}$ as function of frequency for all modes.

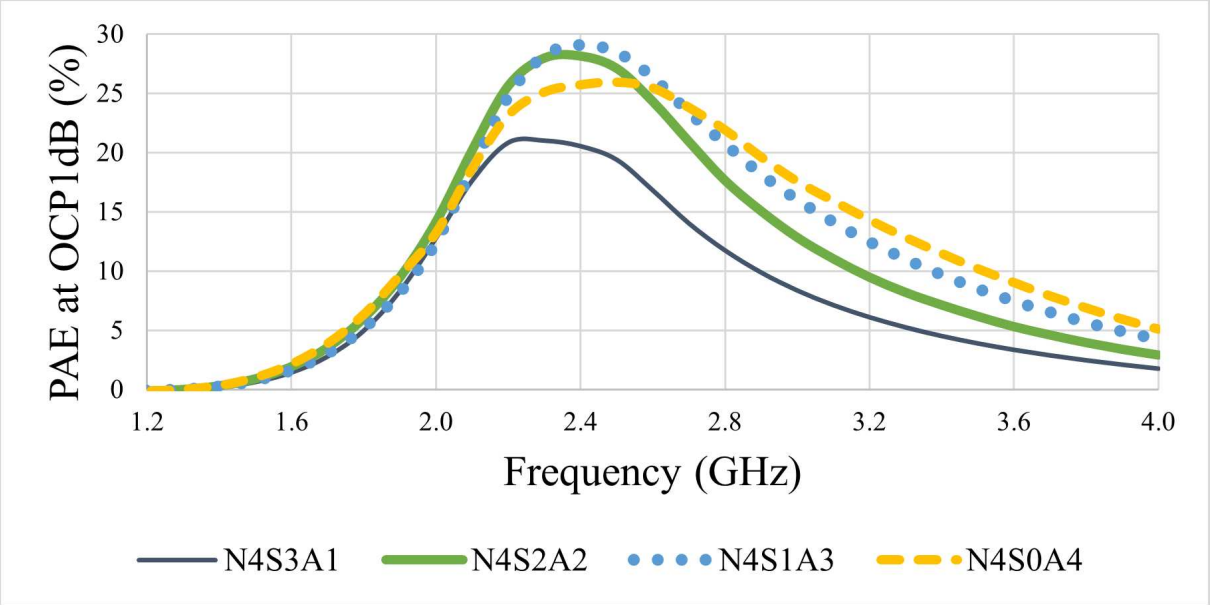


Figure 4.5: PAE at $OCP_{1dB}$ as function of frequency for all modes.

Regarding the S parameters performance, Figure 4.6 presents the $S_{21}$ versus frequency for all four modes. Regarding the 3 dB bandwidth, it ranges between 2.1 GHz and 2.7 GHz (approximately) for N4S0A4 and N4S1A3 modes and between 2.1 GHz and 2.6 GHz (approximately) for N4S3A1 and N4S2A2 modes. At 2.4 GHz, the PA has an $S_{21}$ of 4.1 dB (N4S3A1), 7.0 dB (N4S2A2), 8.5 dB (N4S1A3), and 7.4 dB (N4S0A4). Figure 4.7 presents $S_{11}$ versus frequency curves for each mode. As for $S_{11}$ at 2.4 GHz, N4S3A1 performs -5.0 dB, N4S2A2 -5.7 dB, N4S1A3 -6.2 dB, and N4S0A4 -6.2 dB. $S_{11}$ and $S_{21}$ performances are below those expected from the "schematic-only" version: -26.4 dB and 14.9 dB for N4S0A4 at 2.4 GHz, respectively. This degradation is due to two factors: to the presence of parasitic passives in the IMN and its slight alteration to improve stability.

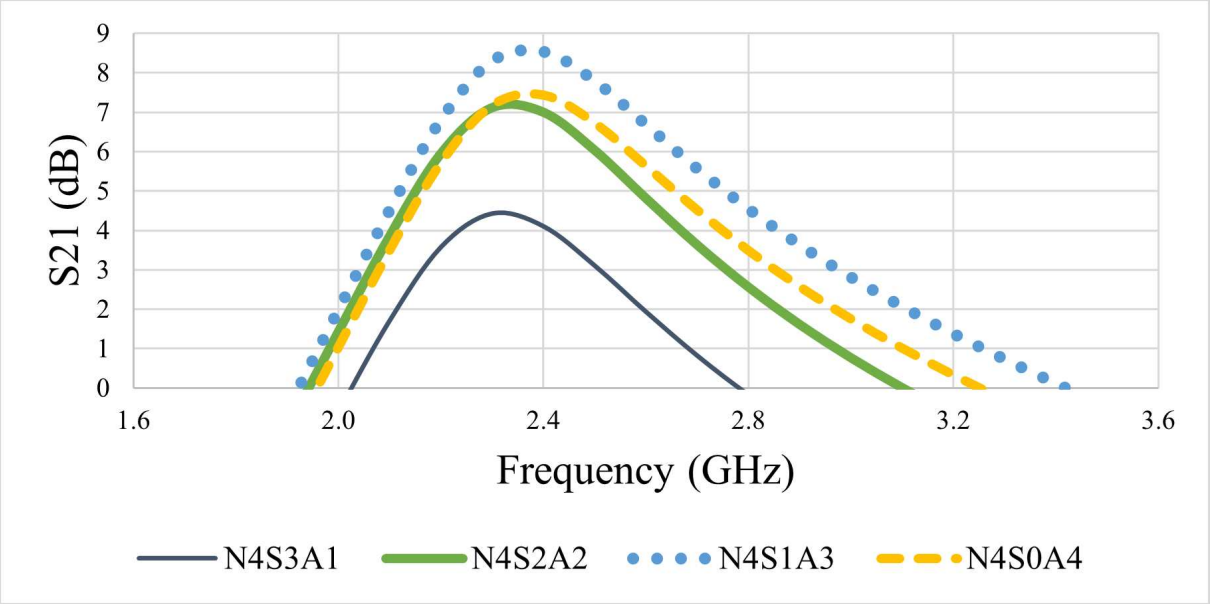


Figure 4.6: $S_{21}$ as function of frequency for all modes.

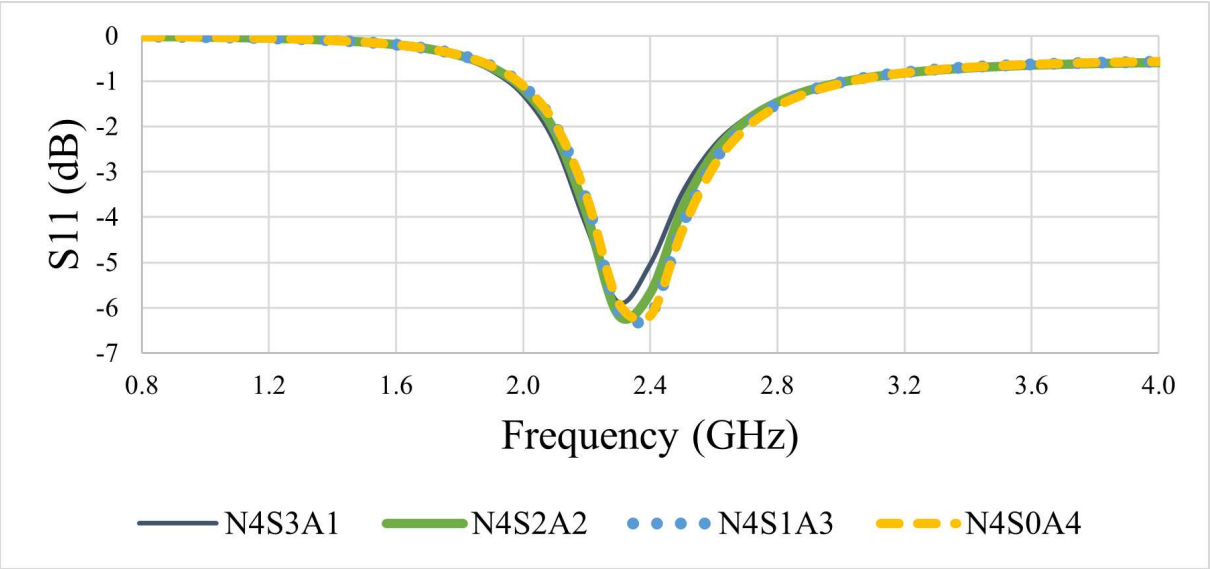


Figure 4.7: $S_{11}$ as function of frequency for all four modes.

## 4.2 PROCESS, VOLTAGE AND TEMPERATURE VARIATIONS RESULTS ON GAIN AND EFFICIENCY

For the PVT analysis, two scenarios were evaluated for each mode: worst (slow-slow corner, 90% of $V_{DD}$, 125 °C) and best (fast-fast corner, 110% of $V_{DD}$, -55 °C). The results obtained from the post-layout simulations are presented in this section.

In Figure 4.8 is presented the power gain curves in function of $p_{out}$ for all modes. The obtained differences between extreme scenarios, considering gain, are: 4.6 dB (N4S3A1), 5 dB (N4S2A2), 7.4 dB (N4S1A3), and 9.0 dB (N4S0A4). In their turn, the differences regarding $OCP_{1dB}$ are: 2.9 dB (N4S3A1), 3.9 dB (N4S2A2), 2.6 dB (N4S1A3), and 2 dB (N4S0A4). As for $p_{peakPAE}$, the difference for N4S3A1 is 3.9 dB, for N4S2A2 is 4.2 dB, for N4S1A3 is 4.7 dB, and for N4S0A4 is also 4.7 dB. Interestingly, even when N4S0A4 is at its worst scenario of operation, its gain curve almost overlaps N4S3A1 at its best, indicating that even under severe degradation (high temperature, low voltage and decreased electron mobility) of operation, mode N4S3A1 may still be used.

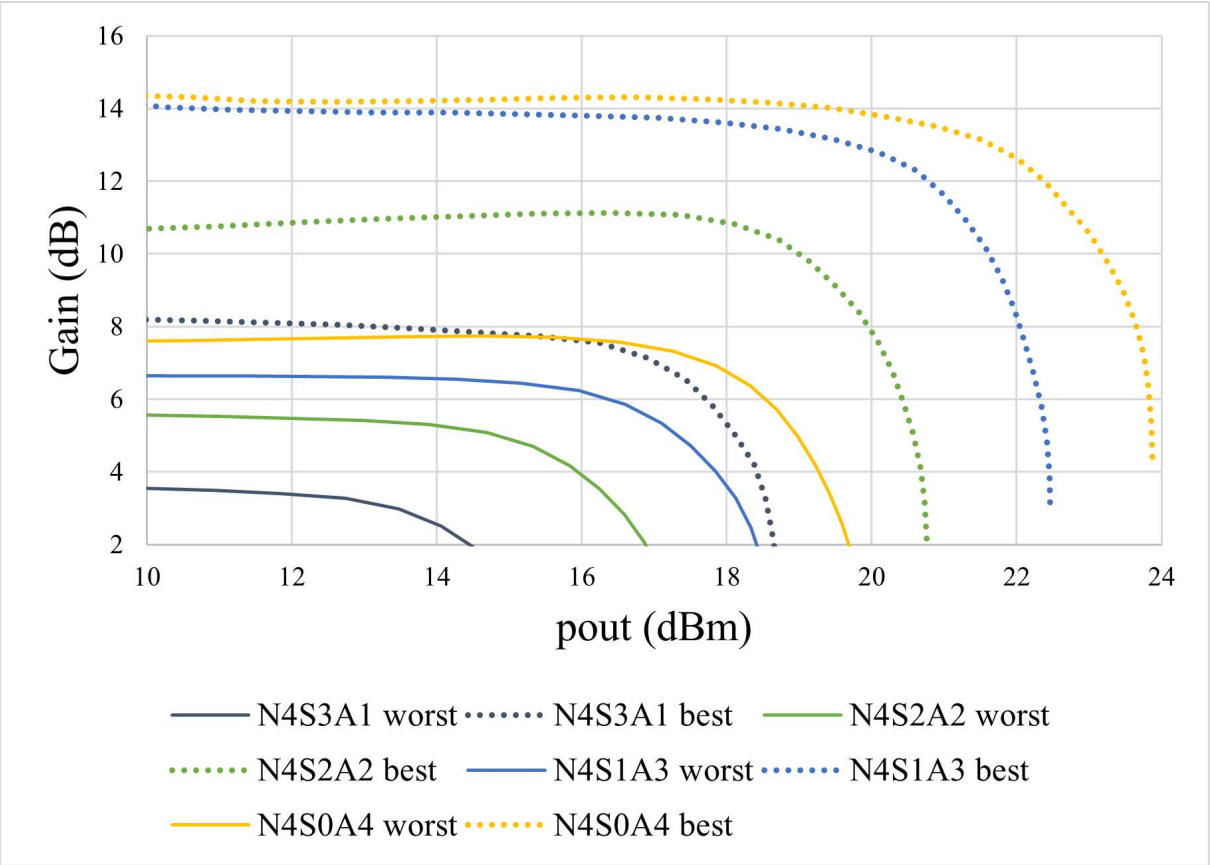


Figure 4.8: Gain as function of $p_{out}$ at 2.4 GHz for all modes operating under worst, typical, and best scenarios.

Finally, in Figure 4.9 is presented the PAE curves in function of $p_{out}$ for all modes. The difference between best and worst scenarios for PAE at $OCP_{1dB}$ are: 15.7 pp (N4S3A1), 20.4 pp (N4S2A2), 14.9 pp (N4S1A3), and 17.1 pp (N4S0A4). Concerning PAE at $p_{sat}$, the differences are: 15.3 pp (N4S3A1), 20.4 pp (N4S2A2), 19.5 pp (N4S1A3), and 16.5 pp (N4S0A4).

All these differences are explained by the increase (fast corner) and decrease (slow corner) of the electron mobility, to the increase or decrease of free electrons concentration (higher and lower temperatures, respectively[3]), and to the supply voltage, which allows a higher or lower gain and output power. The obtained results for the metrics of interest are summarized in Table 4.2.

[3]See equation (1.2.8b) from Tsividis (2013)

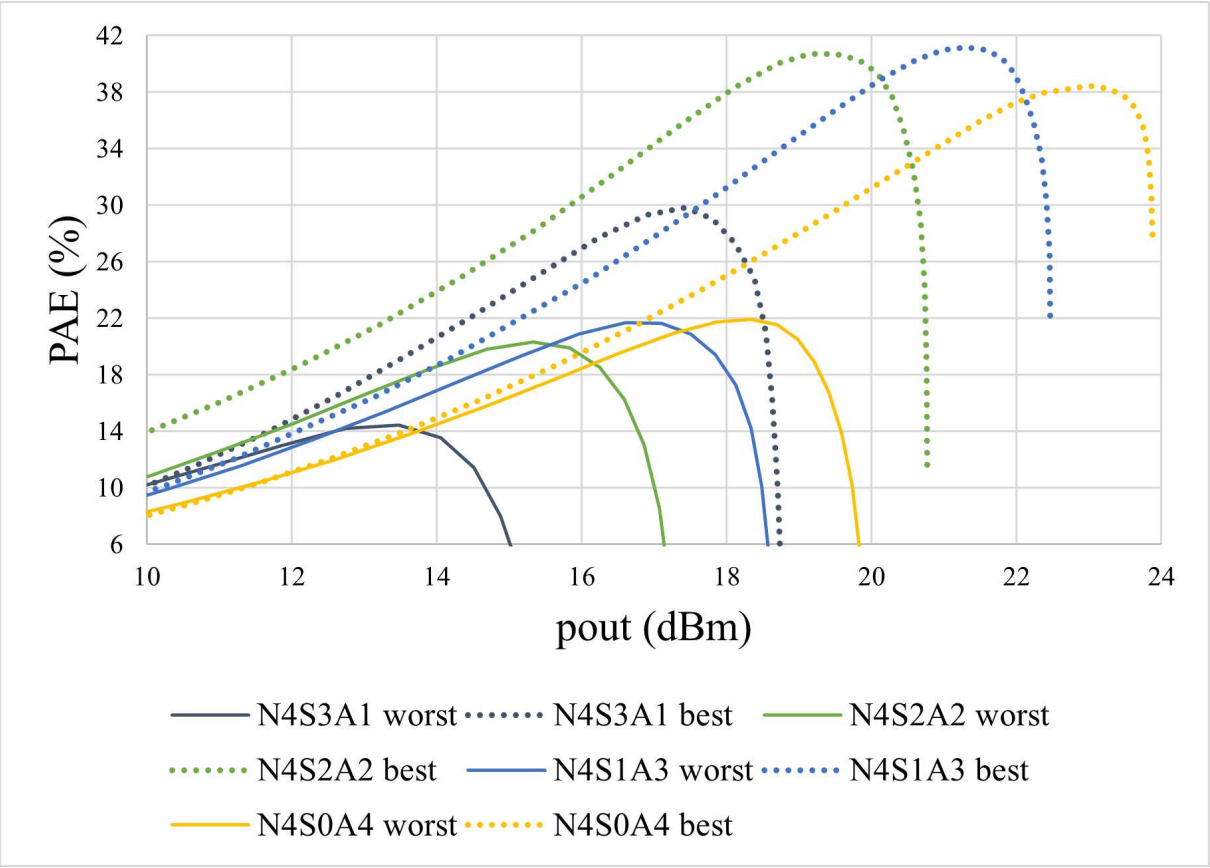


Figure 4.9: PAE as function of $p_{out}$ at 2.4 GHz for all modes operating under worst, typical, and best scenarios.

**Table 4.2** Summary of worst and best scenarios for the selected metrics.

| Mode | Worst | | | | Best | | | |
|---|---|---|---|---|---|---|---|---|
| Mode | N4S3A1 | N4S2A2 | N4S1A3 | N4S0A4 | N4S3A1 | N4S2A2 | N4S1A3 | N4S0A4 |
| $OCP_{1dB}$ (dBm) | 13.9 | 15.4 | 16.7 | 19.2 | 16.8 | 19.3 | 19.3 | 21.2 |
| PAE at $OCP_{1dB}$ (%) | 13.6 | 20.3 | 21.7 | 18.9 | 29.3 | 40.7 | 36.6 | 36.0 |
| $p_{peakPAE}$ (dBm) | 13.5 | 15.3 | 16.6 | 18.3 | 17.4 | 19.5 | 21.3 | 23.0 |
| peak PAE (%) | 14.5 | 20.3 | 21.7 | 21.9 | 29.8 | 40.7 | 41.2 | 38.4 |
| Gain (dB) | 3.8 | 5.8 | 6.9 | 5.5 | 8.4 | 10.8 | 14.3 | 14.5 |

## 4.3 MODULATED SOURCE RESULTS

This section will present the obtained post layout simulation results of the EVM and the Power Spectrum Density (PSD) for all PA's modes with an IEEE 802.11ax modulated wave source. Four different modulation coding schemes (MCS)[4] were selected: 1024 QAM (MCS11), 256 QAM (MCS9), 64 QAM (MCS7), and 16 QAM (MCS4). For each of these scenarios, the source was set to operate with carrier frequency of 2412 MHz, bandwidth of 20 MHz, and guard interval of 0.8 µs. These simulation results were obtained via SpectreRF Wireless Mode in Envelope Analysis, an integrated and automated simulation flow for standard-compliant modulated sources.

Regarding the obtained results for each mode, the EVM values (in dB) were registered as function of $p_{out}$. When the EVM reached the standardized limits (-35 dB for 1024 QAM, -32 dB for 256 QAM, -27 dB for 64 QAM, and -19 dB for 16 QAM), $p_{out_{lim}}$ is defined. At $p_{out_{lim}}$,

[4]MCSs are available at http://mcsindex.com/

PSD as function of frequency is simulated and obtained curves are registered for each mode. The metrics for this final analysis are the Average Main Channel Power (AMCP) and Adjacent Channel Power Ratio (ACPR) at -20 MHz and 20 MHz.

#### *4.3.0.1 IEEE 802.11ax 1024 QAM*

For the 1024 QAM, the EVM limit of -35 dB was reached with a $p_{out_{lim}}$ of 8.5 dBm, 5.0 dBm, 5.8 dBm, and 3.9 dBm for N4S3A1, N4S2A2, N4S1A3, and N4S0A4 modes, respectively (Figure 4.10).

At $p_{out_{lim}}$, all modes fully comply with the mask requirements (Figure 4.11). The AMCPs are: 7.3 dBm (N4S3A1), 5.3 dBm (N4S2A2), 5.7 dBm (N4S1A3), and 4.7 dBm (N4S0A4). Finally, the ACPR at -20 MHz and at 20 MHz are: -36.2 dB and -35.6 dB (N4S3A1), -36.2 dB and -35.6 dB (N4S2A2), -36.2 dB and -35.6 dB (N4S1A3), and -36.1 dB and -35.5 dB (N4S0A4).

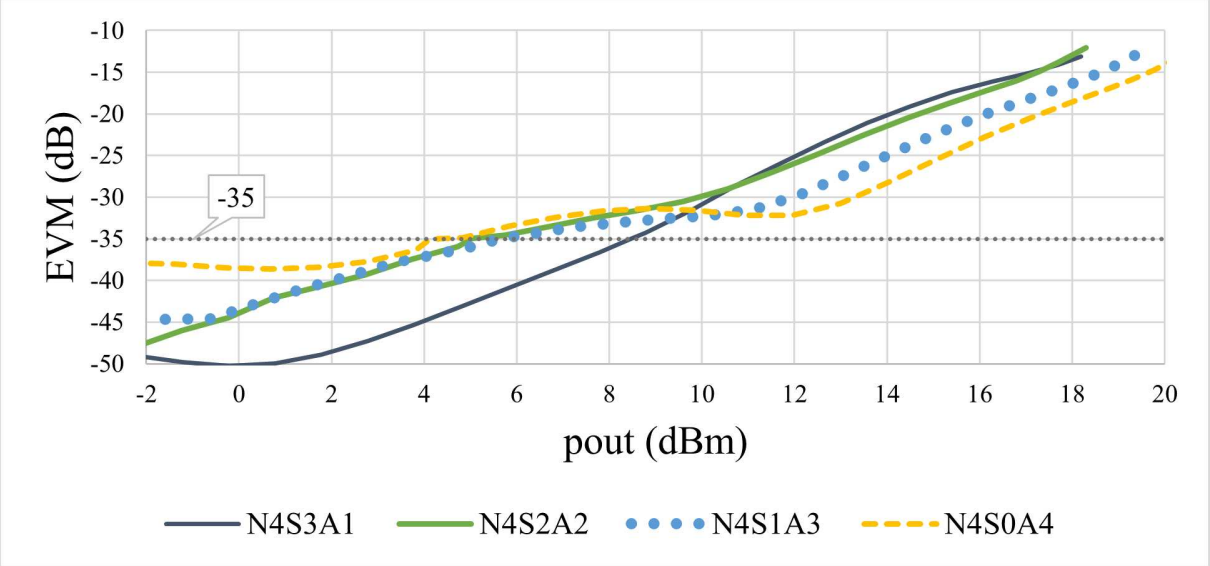


Figure 4.10: EVM as function of $p_{out}$ for all modes operating with a 1024 QAM IEEE 802.11ax source.

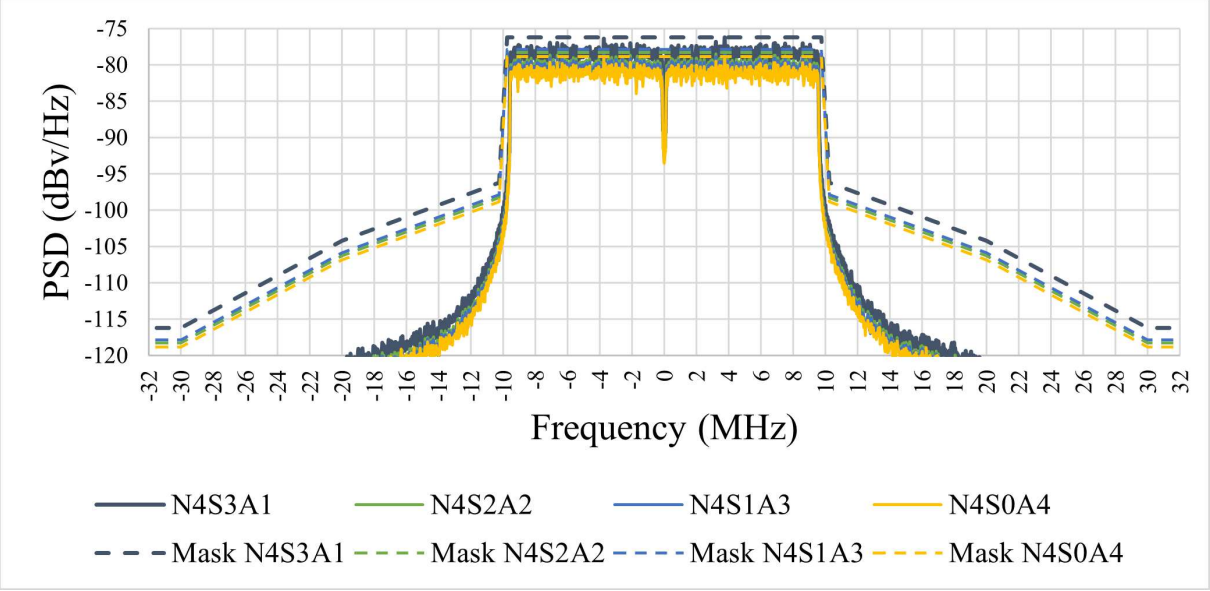


Figure 4.11: PSD as function of frequency for all modes at $p_{out_{lim}}$ for a 1024 QAM IEEE 802.11ax source.

#### *4.3.0.2 IEEE 802.11ax 256 QAM*

As for the the 256 QAM, the EVM limit of -32 dB was reached with a $p_{out_{lim}}$ of 9.6 dBm, 8.2 dBm, 10.4 dBm, and 10.9 dBm for N4S3A1, N4S2A2, N4S1A3, and N4S0A4 modes, respectively (Figure 4.12).

At $p_{out_{lim}}$, all modes fully comply with the mask requirements (Figure 4.13). The AMCPs are: 8.3 dBm (N4S3A1), 8.0 dBm (N4S2A2), 10.3 dBm (N4S0A4), and 10.9 dBm (N4S0A4). Finally, the ACPR at -20 MHz and at 20 MHz are: -34.5 dB and -34.6 dB (N4S3A1), -34.4 dB and -34.6 dB (N4S2A2), -34.2 dB and -34.4 dB (N4S1A3), and -34.0 dB and -34.1 dB (N4S0A4).

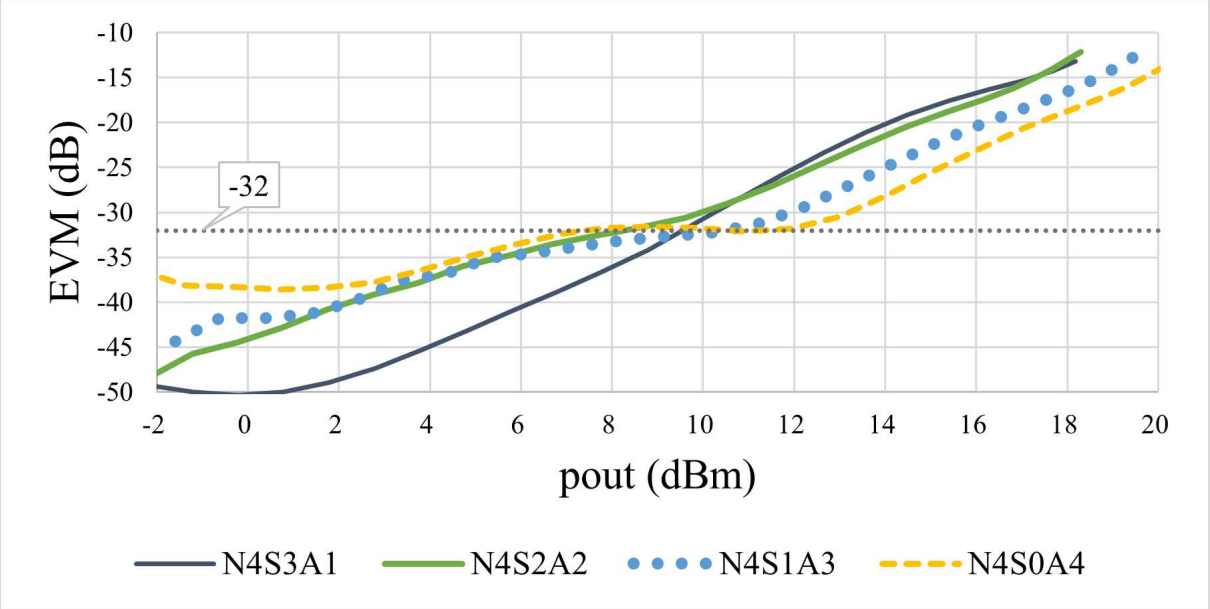


Figure 4.12: EVM as function of $p_{out}$ for all modes operating with a 256 QAM IEEE 802.11ax source.

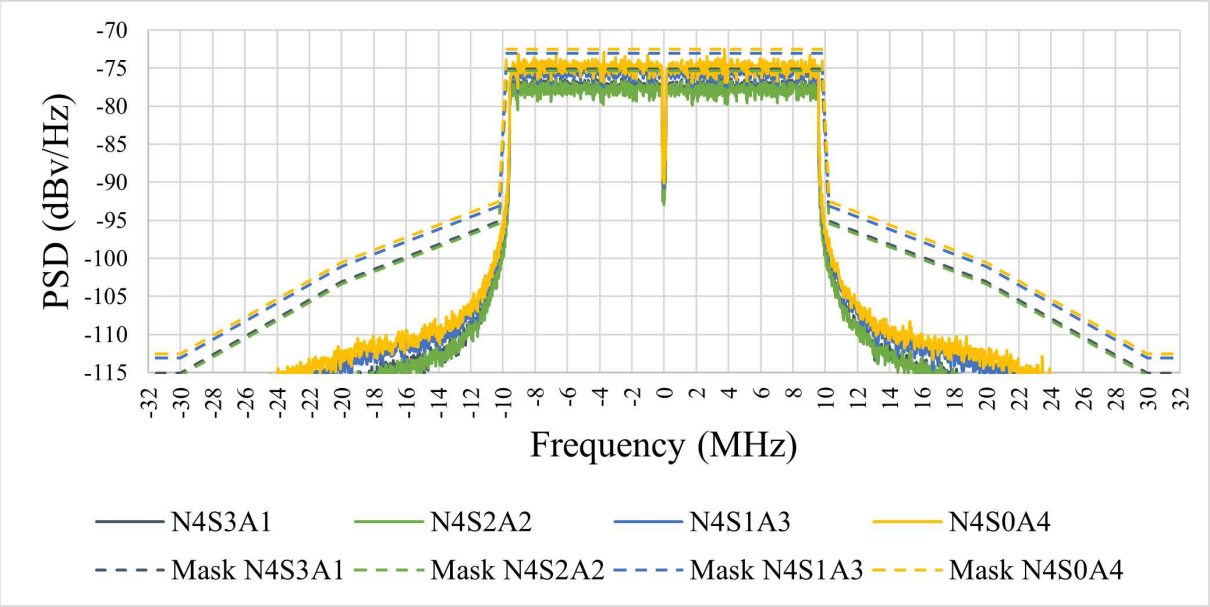


Figure 4.13: PSD as function of frequency for all modes at $p_{out_{lim}}$ for a 256 QAM IEEE 802.11ax source.

#### *4.3.0.3 IEEE 802.11ax 64 QAM*

For the 64 QAM, the EVM limit of -27 dB was reached with a $p_{out_{lim}}$ of 11.3 dBm, 11.5 dBm, 13.2 dBm, and 14.5 dBm for N4S3A1, N4S2A2, N4S1A3, and N4S0A4 modes, respectively (Figure 4.14).

At $p_{out_{lim}}$, all modes fully comply with the mask requirements (Figure 4.15). AMCPs are: 10.0 dBm (N4S3A1), 11.2 dBm (N4S2A2), 12.9 dBm (N4S1A3), and 14.1 dBm (N4S0A4). Finally, the ACPR at -20 MHz and at 20 MHz are -31.6 dB and -31.8 dB (N4S3A1), -31.4 dB and -31.6 dB (N4S2A2), -31.3 dB and -31.4 dB (N4S1A3), and -31.1 dB and -31.2 dB (N4S0A4).

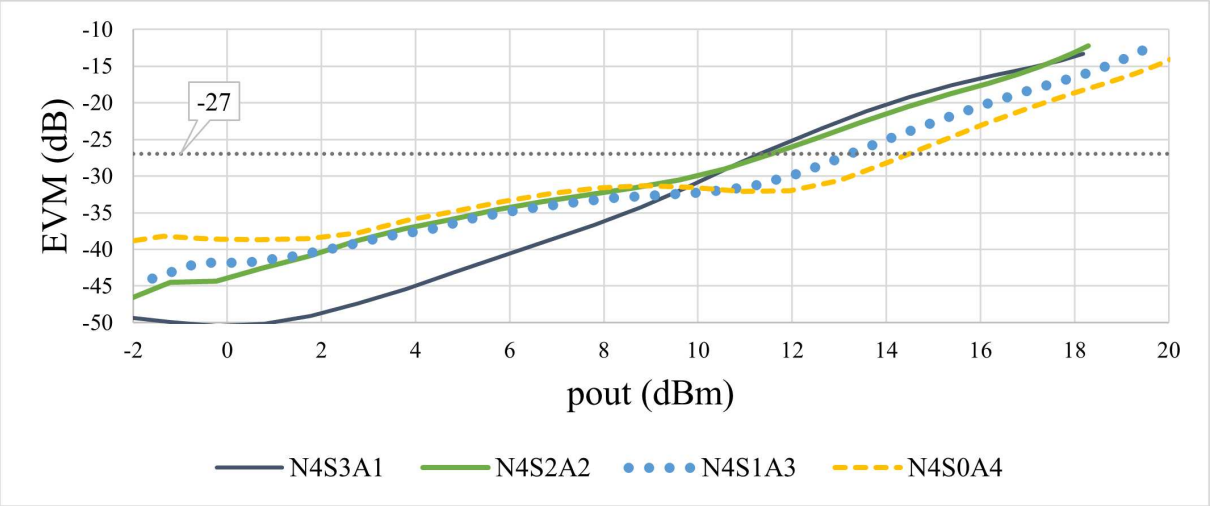


Figure 4.14: EVM as function of $p_{out}$ for all modes operating with a 64 QAM IEEE 802.11ax source.

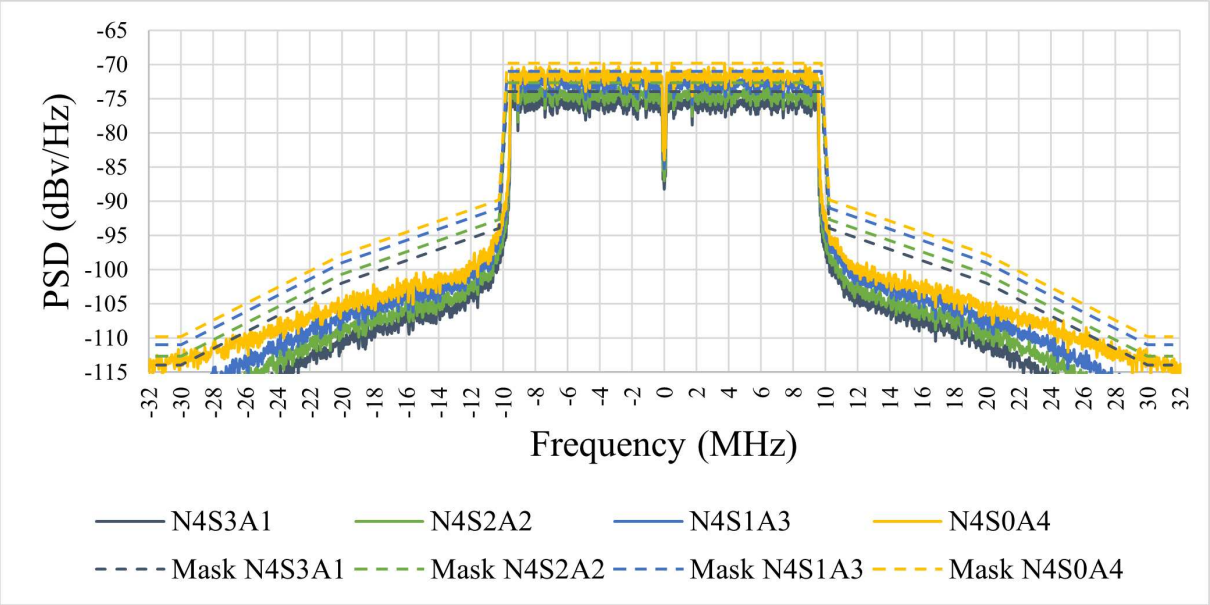


Figure 4.15: PSD as function of frequency for all modes at $p_{out_{lim}}$ for a 64 QAM IEEE 802.11ax source.

#### *4.3.0.4 IEEE 802.11ax 16 QAM*

Finally, for the 16 QAM, the EVM limit of -19 dB was reached with a $p_{out_{lim}}$ of 14.6 dBm, 15.3 dBm, 16.7 dBm, and 17.8 dBm for N4S3A1, N4S2A2, N4S1A3, and N4S0A4 modes, respectively (Figure 4.16).

At $p_{out_{lim}}$, all modes partly comply with the mask requirements (Figure 4.17) as there are some $p_{out}$s between |24| MHz and |18| MHz that exceeds slightly the mask's value. The AMCPs are: 12.7 dBm (N4S3A1), 14.2 dBm (N4S2A2), 15.7 dBm (N4S1A3), and 16.8 dBm (N4S0A4). Finally, the ACPRs at -20 MHz and at 20 MHz are -25.0 dB and -24.9 dB (N4S3A1), -25.0 dB and -24.9 dB (N4S2A2), -24.9 dB and -24.8 dB (N4S1A3), and -25.0 dB and -24.9 dB (N4S0A4).

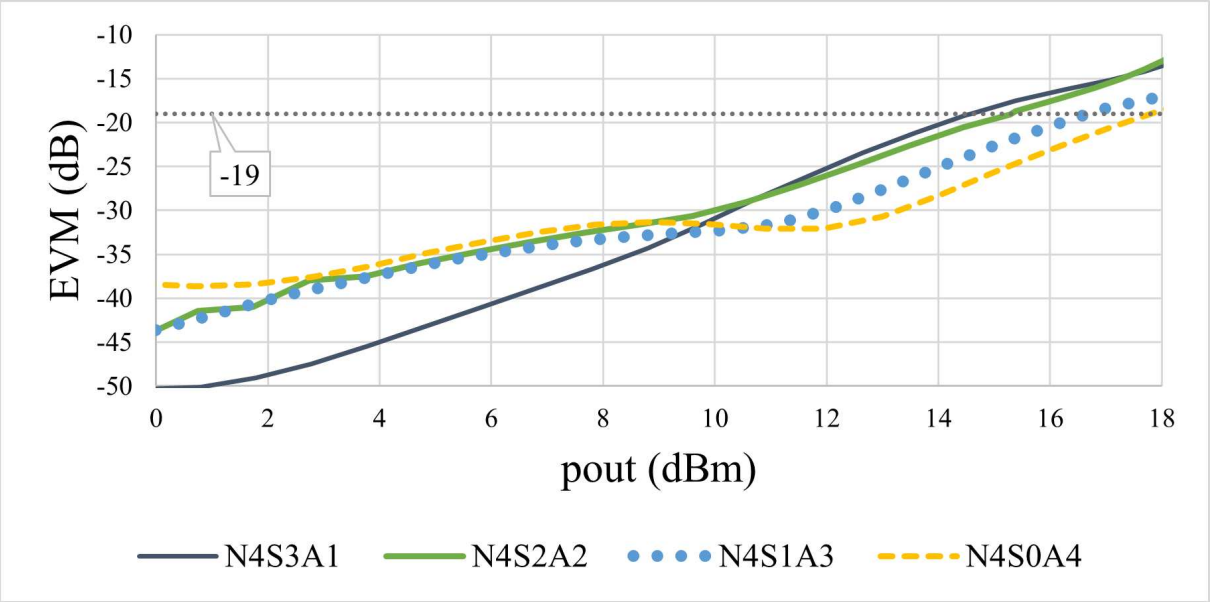


Figure 4.16: EVM as function of $p_{out}$ for all modes operating with a 16 QAM IEEE 802.11ax source.

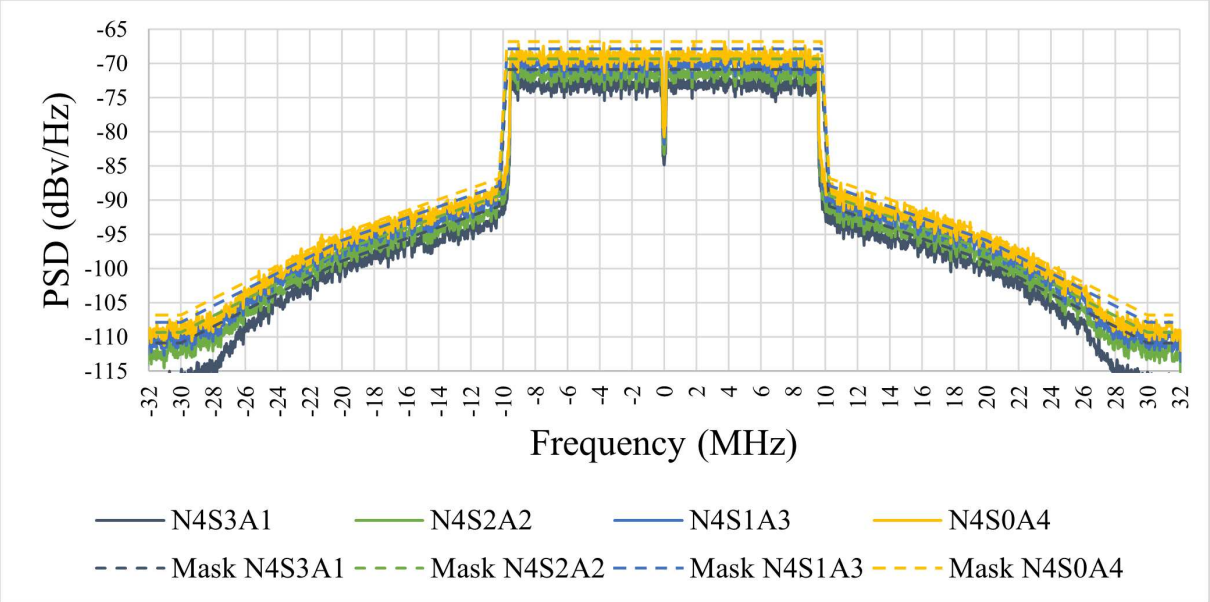


Figure 4.17: PSD as function of frequency for all modes at $p_{out_{lim}}$ for a 16 QAM IEEE 802.11ax source.

A summary of the post-layout results for the evaluated IEEE 802.11ax signals for all modes is presented in Table 4.3. An impressive result is the mode N4S3A1 having a better performance for 1024 QAM than other modes. This difference may be explained by the low power gain this mode has: a low power gain allows the PA to add less error to the transmitted

symbol than it would add if the gain was higher. This characteristic is the trade-off of this mode being unusable under a continuous-wave operation.

**Table 4.3** Summary of the IEEE 802.11ax 1024, 256, 64, and 16 QAM signals for all four modes.

| Modulation | 1024 QAM | | | | 256 QAM | | | |
|---|---|---|---|---|---|---|---|---|
| EVM limit (dB) | -35 | | | | -32 | | | |
| Mode | N4S0A4 | N4S1A3 | N4S2A2 | N4S3A1 | N4S0A4 | N4S1A3 | N4S2A2 | N4S3A1 |
| $p_{out_{lim}}$ (dBm) | 3.9 | 5.8 | 5.0 | 8.5 | 10.9 | 10.4 | 8.2 | 9.6 |
| AMCP (dBm) | 4.7 | 5.7 | 5.3 | 7.3 | 10.9 | 10.3 | 8.0 | 8.3 |
| ACPR (dB) | -36.1, -35.5 | -36.2, -35.6 | -36.2, -35.6 | -36.2, -35.6 | -34.0, -34.1 | -34.2, -34.4 | -34.4, -34.6 | -34.5, -34.6 |
| Modulation | 64 QAM | | | | 16 QAM | | | |
| EVM limit (dB) | -27 | | | | -19 | | | |
| Mode | N4S0A4 | N4S1A3 | N4S2A2 | N4S3A1 | N4S0A4 | N4S1A3 | N4S2A2 | N4S3A1 |
| $p_{out_{lim}}$ (dBm) | 14.5 | 13.2 | 11.5 | 11.3 | 17.8 | 16.7 | 15.3 | 14.6 |
| AMCP (dBm) | 14.1 | 12.9 | 11.2 | 10.0 | 16.8 | 15.7 | 14.2 | 12.7 |
| ACPR (dB) | -31.1, -31.2 | -31.3, -31.4 | -31.4, -31.6 | -31.6, -31.8 | -25.0, -24.9 | -24.9, -24.8 | -25.0, -24.9 | -25.0, -24.9 |

## 4.4 COMPARISON TO THE STATE-OF-THE-ART

A comparison of previously published works is presented in Table 4.4. The compared works are all CMOS based PAs with the same operating frequency of 2.4 GHz (except for Luong et al. (2018) and Haghighat and Nabavi (2016) which operate at 2.5 GHz and 2.6 GHz, respectively) and are placed between 65 nm and 180 nm technology nodes. The lowest employed supply voltage is 1.1 V from Modesto et al. (2019) while the highest is 3.8 V from this work. The following observations account that Luong et al. (2018) and Ou et al. (2017) are data obtained from measurements and that the other works are results from post-layout simulations. Overall, this work stands-out from the presented literature by providing interesting PAE values, specially at N4S2A2 mode (yet, the highest PAE is achieved by Haghighat and Nabavi (2016), 2.6 percentage points higher). It does not employ transformers nor any type of differential structures (as Luong et al. (2018) and Ou et al. (2017) do), is totally single-ended (as Modesto et al. (2019), Santos et al. (2016), and (Haghighat and Nabavi, 2016) are) and has no parallel amplification cores, as all other compared works do.

With regard to the area, this work is more than four times smaller than the PAs proposed by Modesto et al. (2019) and Santos et al. (2016) and eight times smaller than that found in (Luong et al., 2018). Even if pads were added, they would not cause significant increase in area; this result is of special interest because it indicates and reiterates the premise that single-propagation path multimode architectures tend to occupy smaller areas (another example of such trend, measuring 1.5 $mm^2$ under 2.4 GHz operation, is presented in Yin et al. (2014)) than multi-propragation path multimode architectures.

At N4S2A2 mode, it has the highest PAE at $OCP_{1dB}$ and the second highest peak PAE. Specifically, it exceeds by 16.8 percentage points the second highest PAE at $OCP_{1dB}$ (Haghighat and Nabavi, 2016), by almost 11 percentage points the third highest peak PAE, and has 2.6 pp lower than the highest peak PAE. Regarding $OCP_{1dB}$ and $p_{sat}$, this work is 2.4 dB and 5.1 dB lower than Luong et al. (2018), respectively.

At N4S0A4 mode the proposed PA has the second highest PAE at $OCP_{1dB}$ and the third highest peak PAE. This work's N4S0A4 efficiency exceeds by more than 6 percentage points the

third highest PAE at $OCP_{1dB}$ and performs 4.6 percentage points lower than the highest. With regard to the peak PAE, it 0.5 percentage points lower than the peak PAE presented by Luong et al. (2018) and 5.8 pp displayed in Haghighat and Nabavi (2016). Regarding $OCP_{1dB}$ and $p_{sat}$, this work is 1.6 dB and 7.8 dB lower than Luong et al. (2018), respectively.

**Table 4.4** Comparison to the state-of-the-art.

| Reference | Tech. node (nm) | Area ($mm^2$) | $OCP_{1dB}$ (dBm) (min/max) | PAE at $OCP_{1dB}$ (%) (min/max) | $p_{sat}$ (dBm) (min/max)[4] | peak PAE (%) (min/max) | Is differential? |
|---|---|---|---|---|---|---|---|
| Modesto et al. (2019)* | 130 | 1.7 | 10.1/18.2 | 10.6/19.4 | 10.7/18.7 | 13.5/25.0 | No |
| Luong et al. (2018) | 65 | 3.2 | 19.2/21.5[1] | 7.5/8.0[1] | 24.0/29.0[1] | 17.5[1]/26.2 | Yes |
| Ou et al. (2017) | 180 | 2.3 | 11.8/19.1 | 7.0/12.1[1] | 16.0/22.5 | 12.0/19 | Yes |
| Haghighat and Nabavi (2016)* | 180 | 2.9 | 17.2/20.2 | 12.9/30.3 | NA[2]/21[1] | 31.0/31.5[1] | No |
| Santos et al. (2016)* | 130 | 1.7 | 6.0/18.0 | 2.4/16.5 | 8.0/19.0 | 3.8/21.9 | No |
| This work's N4S2A2/N4S0A4* | 130 | 0.4[3] | 16.8/19.9 | 28.1/25.7 | 18.9/21.2 | 28.4/25.7 | No |

*Simulation results. [1]Graphically determined. [2]Not available. [3]Without pads. [4]This work uses $p_{peakPAE}$ instead of $p_{sat}$.

## 4.5 CONCLUSION

This chapter presented the obtained results of the developed proof-of-concept PA. Specifically, the efficiency profiles are N4S0A4 (four transistors operate as amplifiers), N4S1A3 (three transistors operate as amplifiers and one as a switch), N4S2A2 (two transistors operate as amplifiers and two as switches), and N4S3A1 (one transistor operate as amplifier and three as switches). Considering the operation extremes, this PA performs an $OCP_{1dB}$, and PAE at $OCP_{1dB}$ of: 19.9 dBm and 25.7% at N4S0A4 and 15.2 dBm and 20.5% at N4S3A1. Regarding PVT, the PA performs at the worst and best scenarios an $OCP_{1dB}$, and PAE at $OCP_{1dB}$ of: 13.9 dBm and 13.6% (worst N4S3A1) and 19.2 dBm and 18.9% (worst N4S0A4); 16.9 dBm and 29.3% (best N4S3A1) and 21.2 dBm and 36.0% (best N4S0A4). Finally, as for the IEEE 802.11ax, the PA was evaluated in all modes with 1024 QAM, 256 QAM, 64 QAM, and 16 QAM. For every modulation, the modes performed a $p_{out}$ at EVM limit of: 14.7 dBm (N4S3A1), 15.3 dBm (N4S2A2), 16.7 dBm (N4S1A3), and 17.8 dBm (N4S0A4) for 16 QAM; 11.3 dBm (N4S3A1), 11.5 dBm (N4S2A2), 13.2 dBm (N4S1A3), and 14.5 dBm (N4S0A4) for 64 QAM; 9.6 dBm (N4S3A1), 8.3 dBm (N4S2A2), 10.5 dBm (N4S1A3), and 10.9 dBm (N4S0A4) for 256 QAM; and finally, 8.5 dBm (N4S3A1), 6.8 dBm (N4S2A2), 7.0 dBm (N4S1A3), and 5.9 dBm (N4S0A4) for 1024 QAM.

The following chapter will present the final conclusion of this work.

# 5 CONCLUSION

This work aimed to test the hypothesis if a single propagation path single-mode architecture could behave as a multimode arrangement. To verify it, this thesis modified the stacked arrangement to present a single propagation path PA that allows multimode operation, the hybrid. This configuration bases itself on the concept that the consecutive voltage amplifications on a stacked architecture can be chosen to occur or not based on the selection of the stacked transistor's operation region (saturation or triode) and on the scaling of supply voltage. Before the continuous-wave, PVT analysis, and modulated sources post-layout results were presented, an accumulatively theoretical background was discussed and state-of-the-art reviewed, detailing the CS, cascode, stacked, and the hybrid arrangements. This multimode configuration allows the circuit to occupy a small area at cost of a complex optimization process, which is an advantage in scalable CMOS processes. To validate this idea, a four-mode proof-of-concept PA was developed with 130 nm RF CMOS technology measuring 0.4 $mm^2$ (without pads) and verified with IEEE 801.11ax signals. This PA has four efficiency profiles: N4S0A4 (four transistors operate as amplifiers), N4S1A3 (three transistors operate as amplifiers and one as a closed switch), N4S2A2 (two transistors operate as amplifiers and two as closed switches), and N4S3A1 (one transistor operate as amplifier and three as closed switches). Considering the high and low-power modes, this PA performs an $OCP_{1dB}$, and PAE at $OCP_{1dB}$ of 19.9 dBm and 25.7% at N4S0A4 and 15.1 dBm and 20.5% at N4S3A1.

Considering the overall operation, although the proposed circuit achieved four-mode operation, the efficiency profile of N4S3A1 is shadowed by all other modes, especially by N4S2A2, resulting into an effective three-mode PA. This so happened because the initial project requirement was a three-mode PA with more 20 dBm $OCP_{1dB}$ at schematic level simulations - this requirement was met under four stack operation. In this sense, modes N4S0A4, N4S1A3, and N4S2A2 were optimized and enhanced to achieve the best operation possible regarding large-signal continuous-wave metrics and multimode operation. However, considering completeness of this work, it was decided to present all achievable modes and to base all discussions on them. A suggestion to improve efficiency and linearity of mode N4S3A1 is to increase the supply voltage, which could result in a better match of the stack's output impedance with the selected $Z_{loadpull}$. Apart from that, there is also room for improvements in the schematic of presented circuit: adding voltage references for the biasing tree, placing pads and, consequently, re-adjusting the circuit, increasing the number of stacked transistors to achieve even-higher output powers, improving the capacitor bank to reduce the amount of components, adding a gain stage, and improving output matching with a higher order matching network. In terms of layout, this work could also have its area further reduced if the placement and routing were optimized: for example, the amount of spirals and width of the choke inductor could be altered to achieve the needed inductance but vertically placing its input terminal (and not horizontally, as it is).

Regarding future works, a plethora of design possibilities and verification arise from this reconfigurable architecture: the arrangement can be employed in multiband multimode power amplifiers, or even developing PAs in the intermediate inversion region (if the supply voltage and stack height are high enough). If the arrangement is employed in a unitary fashion and these power cells are connected in parallel, a denser power reconfigurability may be achieved (much like enabling or disabling parallel cascode power cells). It is also interesting to understand how the power and gain characteristics of this structure behave in even-higher frequencies of operation, as the $C_{gs}$ and gate capacitors play an important role in the design of the proposed

arrangement. Other interesting possibilities are to understand what are the practical implications in the multimode operation when the stack height is higher than four and how could the hybrid be adjusted to operate in a self-biasing (or in a dynamic biasing) regimen. Finally, another interesting possibility is the usage of such architecture in envelope tracking PAs, which may allow a smoother (while still maintaining highest efficiency) transition among modes. These are only some possibilities of the potential of this architecture. In practice, the hybrid can be used as the power core of many multimode CMOS PAs available in the literature, if adequate adaptations are made.

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